Semiconductor Losses Calculation of a Quasi-Z-Source Inverter with Dead-Time

Original Scientific Paper

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Abstract *– A quasi-Z-source inverter (qZSI) belongs to the group of single-stage boost inverters. The input dc voltage is boosted by utilizing an impedance network and so called shoot-through (ST) states. In pulse-width modulations utilized for the qZSI, the dead-time is commonly omitted. However, unintended ST states inevitably occur as a result of this action, due to the non-ideality of the switching devices, causing the unintended voltage boost of the inverter and an increase in the switching losses. Hence, the implementation of the dead-time is desirable with regard to both the controllability and efficiency of the qZSI. This paper deals with the calculation of semiconductor losses of the three-phase qZSI with implemented dead time. An algorithm available in the literature was utilized for that purpose. The algorithm in question was originally proposed and applied for the qZSI with omitted dead-time, where the occurrence of unintended, undetected ST states combined with the errors in the switching energy characteristics of the insulated gate bipolar transistor (IGBT) provided by a manufacturer led to errors in the obtained results. However, these errors were unjustifiably ascribed solely to the errors in the switching energy characteristics of the IGBT. In this paper, a new, corrected multiplication factor is experimentally determined and applied to the manufacturer-provided IGBT switching energies. The newly-determined multiplication factor is expectedly lower than the one obtained in the case of omitted dead time. The loss-calculation algorithm with the new multiplication factor was experimentally evaluated for different values of the qZSI input voltage, the duty cycle, and the switching frequency.*

Keywords*: dead-time, loss-calculation algorithm, quasi-Z-source inverter, semiconductor losses, switching energies*

NOMENCLATURE

Symbol	Description
C_f	output filter capacitors
C_1, C_2	impedance network capacitors
D_0	shoot-through state duty cycle
D_1	impedance network diode
e_{Dcond}, e_{Drr}	conduction energy and the reverse recovery energy of the free-wheeling diode, respectively
e_{D1cond}, e_{D1rr}	conduction energy and the reverse recovery energy of the impedance network diode, respectively
e_{Tcond}	conduction energy of the transistor
e_{Toff}	turn-off energy of the transistor
e_{Ton}	turn-on energy of the transistor
f_L	frequency of the load voltage
i_{ce}	collector current
i_{D1}	current of the impedance network diode
i_L	current of the impedance network inductor
i_{ph}, I_{ph}	instantaneous value and the RMS value of the phase current, respectively
k_{sw}	multiplication factor
k_T	coefficient representing voltage dependence of transistor switching losses
L_{f1}, L_{f2}	output filter inductors

L_1, L_2	impedance network inductors
m_a	amplitude modulation index
p	non-ST state switching pulses of the transistor
P_{Dcond}	conduction losses of the free-wheeling diode
P_{D1cond}	conduction losses of the impedance network diode
P_{Drr}, P_{D1rr}	reverse recovery losses of the free-wheeling diode and the impedance network diode, respectively
P_{in}	input inverter power
P_L	losses of the impedance network inductors
$P_{measured}$	measured semiconductor losses
P_{out}	output inverter power
P_{Tcond}	transistor conduction losses
P_{Toff}	turn-off losses of the transistor
P_{Ton}	turn-on losses of the transistor
R_{ac}	output load resistance
R_{ce}	forward resistance of the IGBT
R_D, R_{D1}	forward resistance of the free-wheeling diode and the impedance network diode, respectively
R_d	damping resistance
R_g	gate resistance
R_{L1}, R_{L2}	parasitic resistances of the impedance network inductors
ST_{signal}	shoot-through state signal
T_j	junction temperature
T_{sw}	switching period
t_w	energy accumulation time window
T_0	shoot-through state period
V_{ac}	output voltage RMS value
v_{ce}	collector-emitter voltage
$V_{ce,0}$	threshold voltage of the transistor
v_D	voltage across free-wheeling diode
$V_{D,0}$	threshold voltage of the free-wheeling diode
v_{D1}	voltage across impedance network diode
$V_{D1,0}$	threshold voltage of the impedance network diode
v_{in}, V_{in}	Instantaneous value and the mean value of the inverter input voltage, respectively
V_{pn}	peak value of inverter bridge input voltage
V_{ref}	reference voltage
$v_{refA/B/C}$	reference phase voltages
v_{trian}	carrier triangular signal
τ_d	dead-time of the pulse-width modulation

1. INTRODUCTION

The quasi-Z-source inverter (qZSI), proposed in 2008 [1], is a single-stage inverter with boost capability. It represents a modification of an originally proposed Z-source inverter topology, ensuring continuous input current and lower voltage rating of one of the impedance-network capacitors [2]. The impedance network of the qZSI combined with the additional shoot-through (ST) switching state enables boost of the inverter input voltage. During the ST state, the inverter bridge of the qZSI is short circuited, which is forbidden in conventional voltage-source inverters. Therefore, in order to apply conventional pulse-width modulations (PWMs) for the qZSI, the injection of the ST states has to be additionally enabled.

The control of the qZSI is usually achieved by utilizing the sinusoidal PWM (SPWM) or the space-vector PWM (SVPWM), both with the injected ST states. The most common qZSI-compatible SVPWMs, presented in [3], differ by a number of the inverter legs simultaneously utilized for the ST state injection and by a number of the ST state occurrences within a single switching period. The SVPWM with regard to SPWM achieves higher ac voltage at the inverter bridge output for a given input dc voltage. However, this disadvantage of the SPWM may be overcome by injecting 1/6 of the 3rd harmonic component into the respective modulation signals. The qZSI-compatible SPWMs may be divided into two groups. The first comprises SPWMs in which the ST state duty cycle (D_0) is determined by the amplitude modulation index (m_a). The commonly utilized SPWMs in this group are the simple boost control [4], the maximum boost control [4], and the maximum constant boost control [5]. The second group [6-8] comprises SPWMs which allow the D_0 value to vary regardless of the m_a value as long as the D_0 value is lower than the maximum allowed, which is, in turn, defined by the applied m_a value [5]. In [6], the ST state signal is generated based on the comparison of two dc reference signals (positive and negative) with the carrier signal. In this way, the start of the ST state is unsynchronized with the start of the zero-switching PWM state. This results in the additional zero-switching state occurring between the ST state and the preceding active PWM state, which causes additional switching losses. To overcome this problem, a so-called zero-sync SPWM was proposed in [7], where the start of the ST state is synchronized with the start of the zero-switching state. In the same study, an additional unintended voltage boost was noted in the case of the SPWM with omitted dead-time, which is a consequence of the unintended ST states caused by the non-ideality of the utilized transistors. Consequently, it was in [7] proposed to implement the dead-time within the SPWM so as to eliminate the unintended ST states, resulting in the new dead-time zero-sync (DTZS) SPWM.

The power losses of the qZSI consist of the semiconductor losses and passive component losses. The latter include the inductors' losses, which may be determined as in [9, 10], and the capacitors' losses which are generally considered negligible. The calculation of the semiconductor losses represents a challenging task and many methods have been proposed with this regard [11-17]. In [11], the semiconductor losses were calculated based on the measured voltage and current waveforms of the utilized transistors and diodes. This required sensors with high frequency bandwidth due to the fast transients in the current and voltage of the semiconductor devices. On the other hand, in [12-17], the semiconductor losses were calculated based on the characteristics provided by the semiconductor device

manufacturer. In [12], the switching losses were calculated based on the switching energies determined according to the corresponding switching times and the semiconductor device current and voltage. This approach implies linear change of the current and voltage of the semiconductor device during the switching transition. Another possible approach is to utilize the switching energies characteristics [13-17]. These characteristics are defined as a function of the semiconductor current and are typically approximated by utilizing the linear fitting, whereas more accurate approximation is achieved by utilizing the cubic fitting as in [15]. The losses caused by the unintended ST states were not considered in [12-17], but it was observed in [15] that the loss-calculation error increases with the switching frequency, with the transistor switching losses taking up more than 90% of the total semiconductor losses. This was ascribed to the differences between the actual transistor switching energies and those provided by the manufacturer – determined based on the double-pulse test – which may have been caused by the differences between the test circuitry and the utilized laboratory setup, including parasitic capacitance and additional loop resistance/inductance [18]. Consequently, a multiplication factor (k_{sw}) was introduced for the transistor switching energies to minimize the errors between the measured and calculated losses. However, in this way, the losses caused by the unintended ST states were also ascribed to the errors in the switching energy characteristics, resulting in a presumably overestimated value of $k_{sw} = 1.530$.

This paper deals with the calculation of the semiconductor losses of the qZSI with the DTZS SPWM. The loss-calculation algorithm (LCA), originally proposed and denoted LCA2 in [15], is utilized for that purpose. A new experimentally determined k_{sw} value is utilized for the transistor switching energies, following the same procedure as described in [15]. Finally, the semiconductor losses provided by the LCA with the newly-determined k_{sw} are compared with the experimentally obtained values as well as with the values obtained by another, competing algorithm available in the literature.

2. POWER LOSSES OF THE QZSI

The stand-alone qZSI-based control system is shown in Fig. 1. A symmetrical impedance network is considered in this study, i.e. $L_1 = L_2 = L, C_1 = C_2 = C, R_{L1} = R_{L2} = R_L$. The three-phase inverter bridge is composed of six insulated-gate bipolar transistors (IGBTs) with integrated free-wheeling diodes (FWDs). The LCL filter, composed of the inductors (L_{f1}, L_{f2}), capacitors (C_f), and damping resistances (R_d), is connected to the inverter output. The qZSI supplies the three-phase resistive load (R_{ac}), whereas the control system maintains the required RMS value of the fundamental load phase voltage through the adjustment of m_a. The peak value of the inverter bridge input voltage is defined according to the qZSI input voltage (V_{in}) as follows [1]:

$$V_{pn} = \frac{V_{in}}{1-2D_0} = \frac{V_{in}}{1-2\frac{T_0}{T_{sw}}} \quad (1)$$

where T_0 and T_{sw} represent the ST state period and the switching period, respectively, whereas D_0 represents the ST duty cycle.

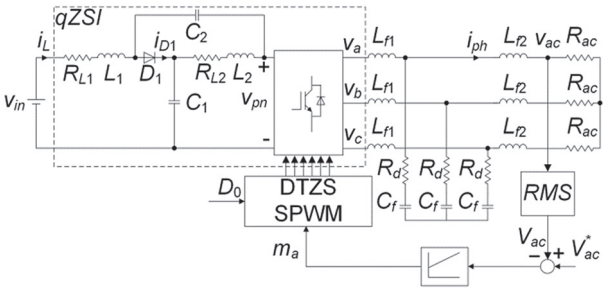

Fig. 1. Stand-alone qZSI-based control system [15]

Fig. 2 shows the waveforms of the reference voltages (v_{refA}, v_{refB}, v_{refC}), the carrier triangular signal (v_{trian}), the ST state signal (ST_{signal}), and the pulses for all the IGBTs (S_{A+}, S_{A-}, S_{B+}, S_{B-}, S_{C+}, S_{C-}) in the case of the DTZS SPWM. The letter in the subscript of "*S*" denotes the corresponding phase, whereas + and – denote the upper and the lower IGBT, respectively. The ST state occurs right at the beginning of each zero-switching state (denoted by the dashed lines). During the ST state, the pulses of all the IGBTs are set to 1. The dead-time (yellow segments) is introduced to postpone the IGBT turn-on pulse ($\tau_d = 0.7$ μs in this study). The considered PWM implied the utilization of the corresponding circuitry, details available in [7].

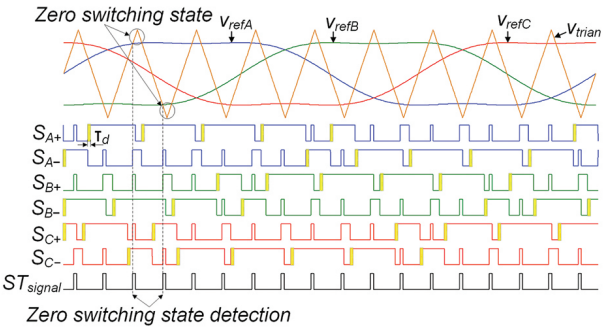

Fig. 2. Waveforms of the dead-time zero-sync SPWM [7]

The power losses of the qZSI represent the difference between the inverter input (P_{in}) and output (P_{out}) powers. These losses include the semiconductor losses and losses of the impedance network inductors and capacitors. The semiconductor power losses are divided into the losses of the IGBTs, the FWDs, and the impedance network diode. As for the IGBTs, the conduction, the switching, and the blocking losses exist, whereas for the diodes the conduction, the reverse recovery, the turn-on, and the reverse losses exist. Generally, the blocking losses of the IGBTs along with the turn-on and reverse losses of the diodes may be considered negligi-

ble. In this study, the semiconductor losses were calculated by utilizing the LCA described in the next section.

3. CALCULATION OF SEMICONDUCTOR LOSSES

The considered LCA was originally applied in [15], where it was denoted LCA2. It enables the calculation of the IGBT and FWD losses in the three-phase inverter bridge and the losses of the impedance network diode. The inverter bridge losses are determined as the losses of a single upper IGBT-FWD pair multiplied by six, based on the assumption of symmetry that holds in the case of the symmetrical output load as is the one utilized in this study. The losses are calculated based on the corresponding energies accumulated in the time window (t_w), as shown in the flow chart in Fig. 3. These energies are obtained from the I–V characteristics and switching energy characteristics of the IGBTs and diodes provided by the semiconductor device manufacturer. The flow chart shown in Fig. 3 may be divided into two parts. The blue-colored part is utilized for the calculation of the IGBT conduction energy accumulated during the ST states and the switching energies of the IGBT and diodes accumulated during the switching transitions between the ST state and the non-ST states. The yellow-colored part of the flow chart shown in Fig. 3 is utilized for the calculation of the energies accumulated during the non-ST states.

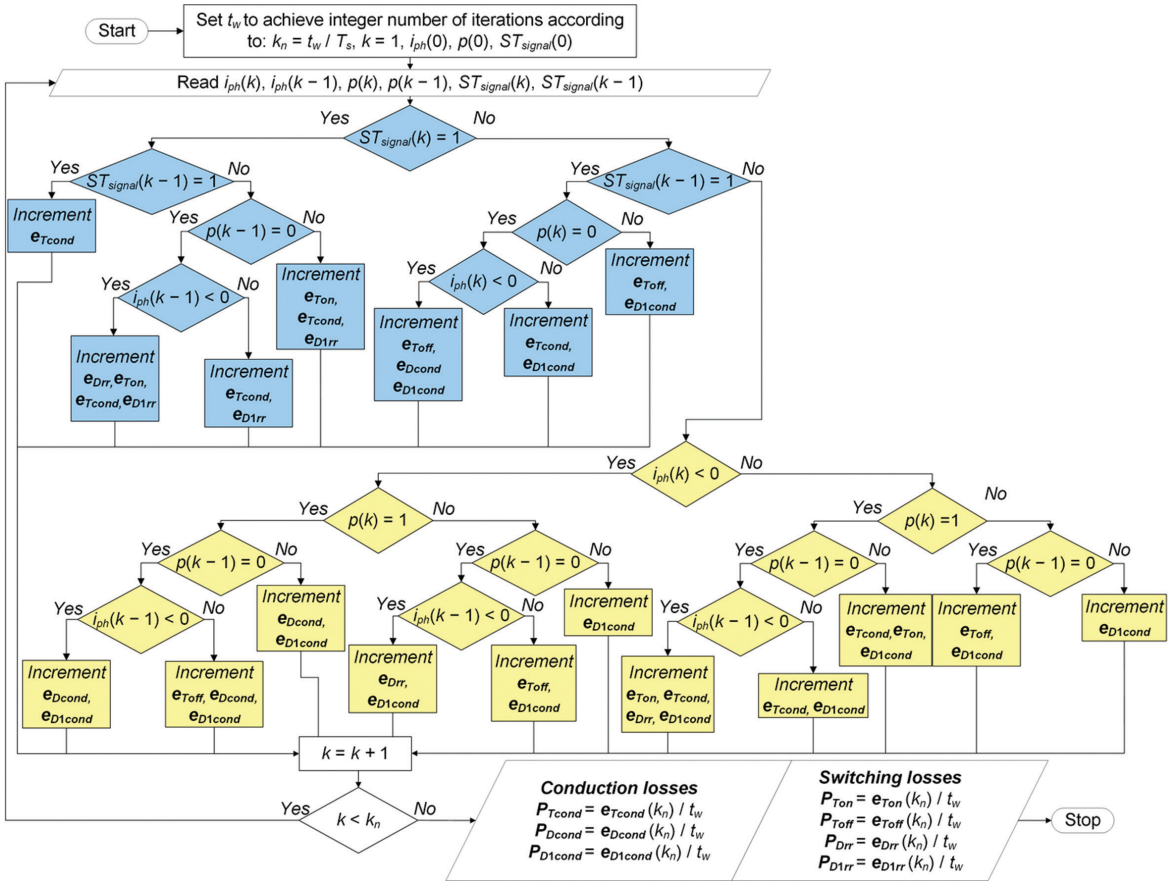

Fig. 3. Flow chart of the LCA [15]

That comprises the conduction and switching energies of the IGBT along with the conduction and reverse recovery energies of the FWD and impedance network diode. The LCA determines which energies should be increased by considering the instantaneous values of the following variables in k^{th} and $(k-1)^{st}$ instants: the non-ST state switching pulses of the IGBT (p), the ST state signal (ST_{signal}), and the phase current (i_{ph}). The IGBT conduction energy (e_{Tcond}) is calculated based on the collector current (i_{ce}) and the collector-emitter voltage (v_{ce}), as follows:

$$e_{Tcond}(k) = e_{Tcond}(k-1) + v_{ce}(k)\left|i_{ce}(k)\right|\left[t(k) - t(k-1)\right]$$
$$v_{ce}(k) = V_{ce,0} + R_{ce}\left|i_{ce}(k)\right| \quad (2)$$

In (2), $V_{ce,0}$ and R_{ce} represent the IGBT threshold voltage and the IGBT forward resistance, respectively (values given in Appendix). During the ST state ($ST_{signal} = 1$), $i_{ce} = 1/2 i_{ph} + 2/3 i_L$, where i_L represents the impedance network inductor current, whereas otherwise $i_{ce} = i_{ph}$.

The conduction energy of the FWD is defined based on the diode forward voltage (v_D) and phase current, as follows:

$$e_{Dcond}(k) = e_{Dcond}(k-1) + v_D(k)\left|i_{ph}(k)\right|\left[t(k) - t(k-1)\right]$$
$$v_D(k) = V_{D,0} + R_D\left|i_{ph}(k)\right| \quad (3)$$

where $V_{D,0}$ and R_D represent the FWD threshold voltage and the FWD forward resistance, respectively (values given in Appendix).

The conduction energy (e_{D1cond}) of the impedance network diode is calculated based on the corresponding threshold voltage ($V_{D1,0}$) and the forward resistance (R_{D1}) (values given in Appendix), as

$$\begin{aligned} e_{D1cond}(k) &= e_{D1cond}(k-1) + \\ &+ v_{D1}(k)\left|i_{D1}(k)\right|\left[t(k)-t(k-1)\right] \\ v_{D1}(k) &= V_{D1,0} + R_{D1}\left|i_{D1}(k)\right| \end{aligned} \quad (4)$$

where v_{D1} and i_{D1} represent the impedance network diode forward voltage and the diode current, respectively.

The IGBT switching losses are calculated based on the corresponding switching energy characteristics. The datasheet of the IGBT-FWD pair utilized in this paper contains the turn-on and turn-off switching energies of the IGBT vs. i_{ce}. These energies are provided for two junction temperatures (T_j = 25 °C and T_j = 150 °C) and for a specific reference value of the inverter bridge input voltage (V_{ref} = 600 V) and the gate resistance (R_g = 10 Ω). Fig. 4 shows the extraction of the characteristics that describe the IGBT turn-on energy (e_{Ton}) vs. i_{ce} by utilizing the cubic fitting. Four coefficients a_0, a_1, a_2, a_3 (values given in Appendix) were obtained by averaging the coefficients obtained for the two provided temperatures. In this study, R_g = 10 Ω was utilized, which corresponds to the value for which the datasheet characteristics were determined.

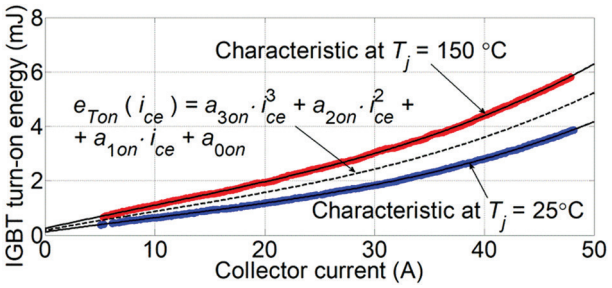

Fig. 4. Turn-on characteristics of the utilized IGBT [15]

The utilized inverter bridge input voltage (V_{pn}) differs from V_{ref} in the datasheet. Therefore, the calculated IGBT turn-on energy was scaled by the ratio $(V_{pn}/V_{ref})^{k_T}$, according to the recommendations in [19], where k_T is the exponent representing the voltage dependance of the IGBT switching losses ranging from 1 to 1.4. Note that the V_{pn} value is determined based on the V_{in} value, as per (1). Finally, by considering all the facts mentioned above, e_{Ton} is obtained as follows:

$$e_{Ton}(i_{ce}) = k_{sw}\left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(a_3 i_{ce}^3 + a_2 i_{ce}^2 + a_1 i_{ce} + a_0\right) \quad (5)$$

In (5), k_{sw} represents a multiplication factor, initially set to 1, introduced to correct the IGBT switching energies, as described in Introduction.

The IGBT turn-off characteristics were extracted in the same way as the turn-on characteristics. The corresponding polynomial is defined as follows:

$$e_{Toff}(i_{ce}) = k_{sw}\left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(b_3 i_{ce}^3 + b_2 i_{ce}^2 + b_1 i_{ce} + b_0\right) \quad (6)$$

where values of b_0, b_1, b_2, b_3 are given in Appendix.

The cumulative values of e_{Ton} and e_{Toff}, obtained based on the flow chart shown in Fig. 3, are calculated as follows:

$$e_{Ton/off}(k) = e_{Ton/off}(k-1) + e_{Ton/off}\left(\left|i_{ce}(k)\right|\right) \quad (7)$$

The reverse recovery energies of the FWD (e_{Drr}) and the impedance network diode (e_{D1rr}) are calculated as follows:

$$e_{Drr}(k) = e_{Drr}(k-1) + e_{Drr}\left(\left|i_{ph}(k)\right|\right) \quad (8)$$

$$e_{D1rr}(k) = e_{D1rr}(k-1) + e_{D1rr}\left(\left|i_{D1}(k)\right|\right) \quad (9)$$

Note that, e_{Drr} and e_{D1rr} utilized in (8) and (9), respectively, are given in Appendix.

4. EXPERIMENTAL INVESTIGATION

Fig. 5 shows the laboratory setup of the stand-alone qZSI-based system. The same measurement equipment and the same sampling procedure as in [15] were utilized for the LCA implementation. Other details about the utilized experimental setup are given in [15].

The measured semiconductor losses ($P_{measured}$) were obtained as $P_{in} - P_{out} - P_L$. The input inverter (P_{in}) power was obtained as the mean value of $v_{in}\cdot i_L$, whereas the output inverter power (P_{out}) was measured by means of the power analyzer Norma 4000 (Fluke). The losses of the inductors (P_L) were calculated as in [9], whereas the losses of the utilized polypropylene capacitors were neglected due to the low ESR value of 7.8 mΩ

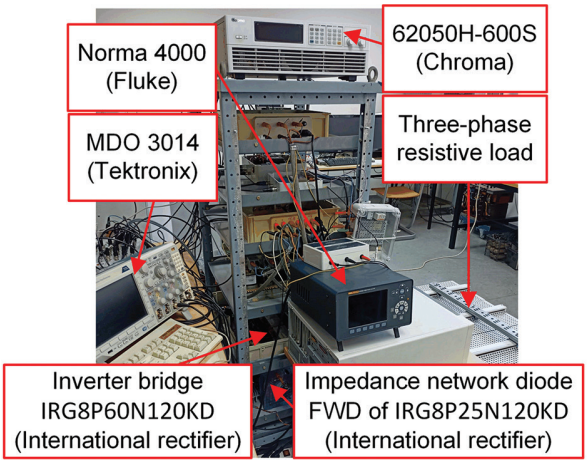

Fig. 5. Laboratory setup of the stand-alone qZSI-based system

4.1 DETERMINATION OF THE MULTIPLICATION FACTOR

The first part of the investigation was carried out to determine the new k_{sw} value applicable for the qZSI

with the DTZS SPWM. For that purpose, the same procedure as in [15] was utilized. The following I_{ph} values were considered: 1.33 A, 1.72 A, 2.12 A, and 2.61 A. During the measurements, f_{sw} and D_0 were set to 5 kHz and 0.22, respectively, whereas V_{in} was set to 450 V, resulting in the constant V_{pn}/V_{ref} ratio with $V_{pn} \approx 800$ V. The reference RMS value (V^*_{ac}) and frequency (f_L) of the fundamental load phase voltage were set to 230 V and 50 Hz, respectively.

The IGBT switching energies were multiplied by k_{sw} to annul the LCA error with respect to $P_{measured}$ for each of the considered I_{ph} values. In this way, the k_{sw} values in the range 1.09 – 1.34 were obtained. The final average value of k_{sw} was calculated as 1.197. As expected, due to the elimination of the unintended ST states and thus the corresponding losses, the new k_{sw} value is about 22% lower than the value previously obtained in [15]. The fact that the new k_{sw} value is still higher than zero speaks in support of the hypothesis that the datasheet values of e_{Ton} and e_{Toff} may differ from the actual ones, as stated in [15]. Note that during the experimental investigation, k_T in (5) and (6) was set to 1.4, which is the highest recommended value [19]. The lower k_T value would result in the higher k_{sw} value.

The comparison between the LCA prior and after the correction of the IGBT switching energies and the measured semiconductor losses is shown in Fig. 6 (left column).

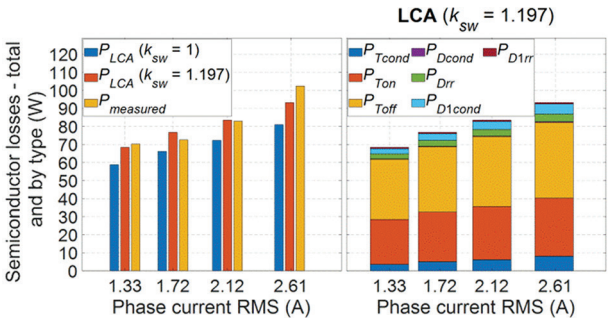

Fig. 6. Measured and calculated semiconductor losses with respect to RMS phase current

In comparison to the results given in [15], the absolute error of the LCA with k_{sw} = 1 (i.e., before the correction) is reduced by approximately 30% solely due to the dead-time implementation. After the application of the corrected factor k_{sw} = 1.197, the highest absolute error was further reduced from 22 W (21%) to 6 W (6%). Note that the error remaining after the correction is probably not related to the conduction losses calculation error, which depends on the chosen LCA sampling period. In this study, the sampling period is set to 2 µs since it has been shown in [15] that the additional reduction of the LCA sampling period does not enhance the LCA's accuracy. The introduced dead-time does not interfere with the LCA's operation because the LCA input variable p represents the actual switching pulses with implemented dead-time.

The right column in Fig. 6 shows the semiconductor losses distribution of the LCA with the applied k_{sw} value of 1.197. The turn-on (P_{Ton}) and turn-off (P_{Toff}) losses of the IGBTs are dominant with the share higher than 90% in the total semiconductor losses. These losses are followed by the conduction losses of the IGBTs (P_{Tcond}) and the conduction losses of the impedance network diode (P_{D1cond}) and FWDs (P_{Dcond}). The reverse recovery losses of FWDs (P_{Drr}) and the impedance network diode (P_{D1rr}) have the lowest share in the total semiconductor losses.

4.2 EXPERIMENTAL EVALUATION OF THE LCA

The second part of the investigation was carried out to evaluate the LCA with the applied k_{sw} in operation ranges that result in different distribution of the semiconductor losses. The semiconductor losses were also calculated by means of another algorithm proposed in [15], where it was denoted LCA1. The corresponding IGBT switching energies were also multiplied by k_{sw} = 1.197.

Fig. 7 shows the corrected calculated and measured semiconductor losses with respect to the switching frequency (f_{sw}), the qZSI input voltage (V_{in}), and the duty cycle (D_0).

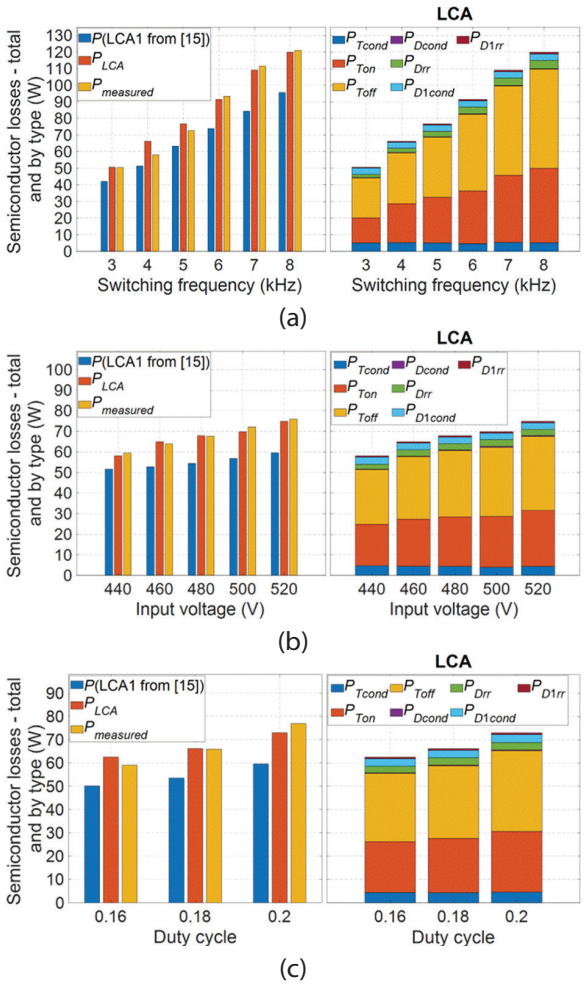

Fig. 7. Corrected calculated (*ksw* = 1.197) and measured semiconductor losses with respect to: switching frequency (a), input voltage (b), and duty cycle (c)

The measurements carried out for this purpose corresponded to the measurements carried out in [15]. The only difference was the utilization of the DTZS SPWM instead of the zero-sync SPWM with omitted dead-time. V_{ac}^{*} and f_L were set to 230 V and 50 Hz, respectively. During the variation of the switching frequency, other parameters were set to the constant values: $D_0 = 0.22$, $I_{ph} = 1.72$ A, $V_{in} = 450$ V. Similarly, the switching frequency was set to 5 kHz when the values of V_{in} and D_0 were varied. The variation of V_{in} was carried out with $D_0 = 0.18$ and $I_{ph} = 1.72$ A, whereas the variation of D_0 was carried out with $I_{ph} = 1.72$ A, $V_{in} = 470$ V. Note that during the variation of V_{in}, the utilization of $D_0 = 0.18$ ensured the highest tolerable V_{pn} value (including transients), which is lower than the maximum allowed value of 1200 V. For the same reason, V_{in} was set to 470 V during the variation of D_0.

The left columns in Fig. 7 indicate that the accuracy of the LCA1 from [15] is lower for all the considered measurement points, with the highest noted error amounting to 25 W (23%), compared to only 9 W (12%) by the LCA. The semiconductor losses distribution of the LCA with the applied $k_{sw} = 1.197$ is shown in Fig. 7 (right columns). This distribution corresponds to the distribution shown in Fig. 6, with dominant P_{Ton} and P_{Toff}.

The second part of the investigation was carried out in order to evaluate the LCA over wide ranges of V_{in} and D_0. The main aim was to consider qZSI applications where V_{in} and V_{pn} vary significantly, such as in the case of a photovoltaic-fed qZSI. In this part of the investigation, the m_a value was set to 0.8, meaning that the output voltage was not controlled, whereas the output load resistance (R_{ac}) was adjusted to maintain 1 kW output power (P_{out}).

Fig. 8 shows the measured and calculated semiconductor losses with respect to V_{in} for the D_0 values of 0.1, 0.15, 0.2, and 0.25.

The results shown in the left columns in Fig. 8 indicate that the semiconductor losses obtained by the LCA (P_{LCA}) closely correspond to the measured losses ($P_{measured}$), with the highest noted error amounting to 11 W (12%). The accuracy of the LCA1 from [15] is lower for all the measurement points, with the highest noted error amounting to 27 W (30%). These results confirm the superior accuracy of the LCA, as previously observed in [15].

The semiconductor losses distribution of the LCA depends on the V_{in} value. In the case of $V_{in} = 200$ V, the conduction losses amount to approximately 60% of the total semiconductor losses for $D_0 = 0.1$. The increase in V_{in} or D_0 causes the increase in V_{pn}, as per (1), and thus the increase in the load voltage due to the constant m_a. Since P_{out} is controlled, higher load voltage implies lower load current and thus lower current through the semiconductors. Therefore, the share of the conduction losses in the total semiconductor losses decreases with the increase in V_{in} or D_0. On the other hand, the share of the switching losses, especially P_{Ton} and P_{Toff}, notably increases with V_{in} and D_0 due to the increase in V_{pn}, as per (1). For example, in the case of applied $V_{in} = 470$ V and $D_0 = 0.25$ the IGBT switching losses amount to 87% of the total semiconductor losses.

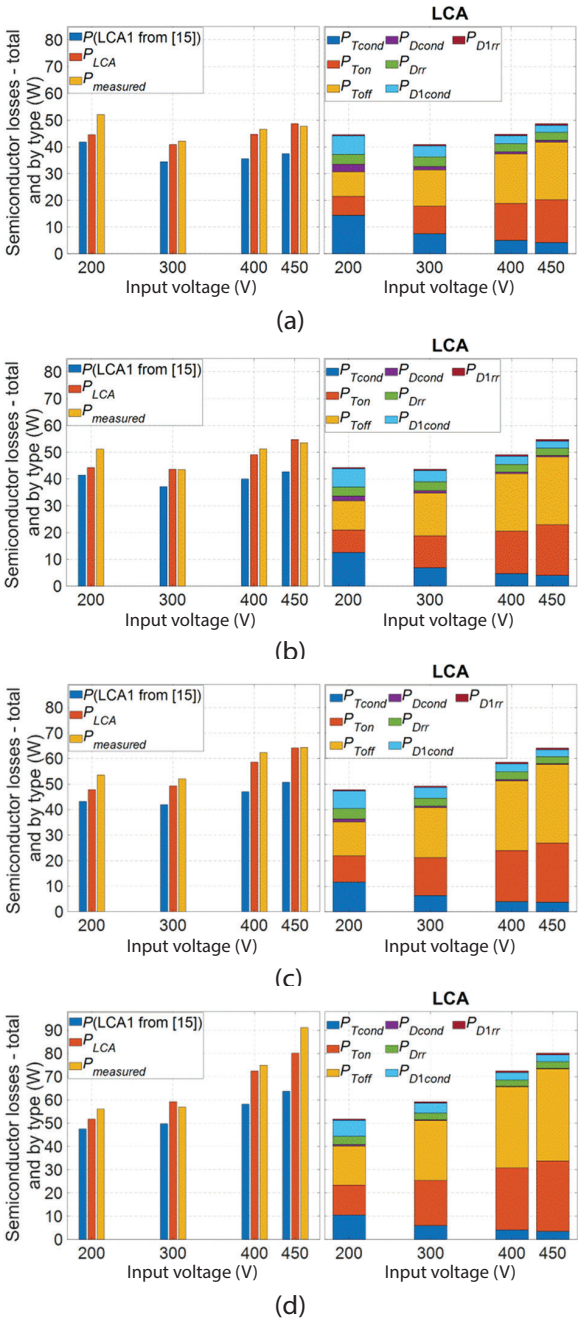

Fig. 8. Corrected calculated ($k_{sw} = 1.197$) and measured semiconductor losses with respect to input voltage for duty cycles of: 0.1 (a), 0.15 (b), 0.2 (c), 0.25 (d)

5. CONCLUSION

In this study, the LCA available in the literature has been successfully applied for the qZSI with the DTZS SPWM. The implementation of the dead-time did not interfere with the LCA's operation, whereas it caused the decrease of the actual inverter losses. As a result, the

corrective multiplication factor for the IGBT switching energies was reduced from 1.530 (omitted dead-time) to 1.197 (implemented dead-time). However, the fact that the new multiplication factor is still different from 1 supports the hypothesis that, in some cases, the manufacturer-provided IGBT switching energies need to be adjusted. Also note that the highest recommended value was utilized for the scaling factor that describes the voltage dependence of the IGBT switching losses. Any reduction of this factor would require higher multiplication factor. Finally, the LCA was experimentally evaluated and compared to another algorithm available in the literature, with the same multiplication factor applied for both the considered algorithms. It turned out that the LCA is overall more accurate with the relative error not exceeding 12%, as opposed to the 30% obtained for the considered competing algorithm.

6. APPENDIX

Parameters and coefficients in (2)-(6)

$R_{ce} = 0.066105\ \Omega$, $V_{ce,0} = 0.6823\ \text{V}$, $R_D = 0.0862\ \Omega$

$V_{D,0} = 0.774\ \text{V}$, $R_{D1} = 0.1225\ \Omega$, $V_{D1,0} = 0.999\ \text{V}$

$a_0 = 0.18$, $a_1 = 0.074$, $a_2 = -7.2 \cdot 10^{-4}$, $a_3 = 2.53 \cdot 10^{-5}$

$b_0 = 0.258$, $b_1 = 0.081$, $b_2 = -1.41 \cdot 10^{-4}$, $b_3 = 0$

Reverse recovery energies in (8), (9)

$$e_{Drr}(i_{ph}) = \left(\frac{V_{pn}}{600}\right)^{0.6} \begin{pmatrix} 9.9 \cdot 10^{-7} i_{ph}^3 - 3.76 \cdot 10^{-4} i_{ph}^2 + \\ + 0.04 i_{ph} + 0.036 \end{pmatrix}$$

$$e_{D1rr}(i_{D1}) = \left(\frac{V_{pn}}{600}\right)^{0.6} \begin{pmatrix} 5.34 \cdot 10^{-6} i_{D1}^3 - 0.0012 i_{D1}^2 + \\ + 0.052 i_{D1} + 0.0145 \end{pmatrix}$$

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