Design of High-Speed Dual Port 8T SRAM Cell with Simultaneous and Parallel READ-WRITE Feature

Original Scientific Paper

Shourin Rahman Aura
Lecturer, Department of Electrical and Electronic Engineering
Ahsanullah University of Science and Technology, Dhaka, Bangladesh
aura.eee@aust.edu

S. M. Ishraqul Huq
Assistant Professor, Department of Electrical and Electronic Engineering
Ahsanullah University of Science and Technology, Dhaka, Bangladesh
Ishraqulhuq.eee@aust.edu

Satyendra N. Biswas
Professor, Department of Electrical and Electronic Engineering
Ahsanullah University of Science and Technology, Dhaka, Bangladesh
sbiswas.eee@aust.edu

Abstract *– An innovative 8 transistor (8T) static random access memory (SRAM) architecture with a simple and reliable read operation is presented in this study. LTspice software is used to implement the suggested topology in the 16nm predictive technology model (PTM). Investigations into and comparisons with conventional 6T, 8T, 9T, and 10T SRAM cells have been made regarding read and write operations' delay and power consumption as well as power delay product (PDP). The simulation outcomes show that the suggested design offers the fastest read operation and PDP optimization overall. Compared to the current 6T and 9T topologies, the noise margin is also enhanced. Finally, the comparison of the figure of merit (FoM) indicates the best efficiency of the proposed design.*

Keywords*: SRAM, CMOS, dual port, figure of merit*

1. INTRODUCTION

Low power and high-speed integrated circuits (ICs) are continually in demand for portable applications such as mobile phones and laptops since high power dissipation reduces the battery life of electronic devices [1, 2]. For its superior performance in terms of the aforementioned metrics, static random-access memory (SRAM) is typically favored over dynamic RAM (DRAM), which requires frequent refreshing, to be employed in cache memories [3, 4]. The growth of the IC industry has led to the aggressive scaling of transistors to increase package density for low chip-area requirements [5]. Consequently, the size of SRAM circuits has decreased significantly [6]. As a result, power dissipation has become a growing concern while designing SRAMs in nanometer technology [7]. The two major operations, read and write, drive the performance of an SRAM cell and, therefore, the factors taken into consideration for design are the dynamic power consumption and latency during these two operations [8]. Dynamic power is the power consumption when the SRAM cell reads or writes any data, and is the major contributor to power consumption in a circuit [9].

A traditional SRAM cell consists of cross-coupled complementary metal-oxide semiconductor (CMOS) inverters, each storing complementary outputs [10]. The storage nodes are accessed using pass-transistors for write, and sometimes read, operations. Existing 6T [11], 8T [12], 9T [13], and 10T [14] SRAM cells require pre-charging of the bit-lines (BL), or read bit-line (RBL) in some cases, during read operation and based on the stored values, one of the bit-lines is discharged. This pre-charging process requires additional circuitry and increases the read delay of the SRAM cell. Moreover, the existing circuits do not allow simultaneous read and write operations. Researchers have also proposed a load-less 4T [15] SRAM circuit to reduce transistor count and power penalty. However, the cell is highly unstable as the voltage level of one of the storage nodes degrades over time. There is no pull-up transistor to charge and hold the storage

nodes to the logic high supply rail. Budhaditya et. al. [16] presented a 5T SRAM cell which eliminates one access transistor to reduce power consumption and chip area. It facilitates the read operation as only one bit-line is pre-charged, thus, reducing read power dissipation. Nevertheless, the 5T circuit lacks a separate read circuit.

This study presents a modified 8T SRAM cell using the 5T write circuit and a CMOS inverter for a separate and isolated read operation. The objective of the proposed circuit is improved read operation with a simultaneous read-write feature.

2. LITERATURE REVIEW

The conventional 6T SRAM cell consists of two CMOS inverters cross-linked with two pass transistors connected to complimentary bit-lines, as shown in Fig. 1. The gates of access transistors M3 and M4 are connected to the write-line (WL), which enables write and read operations to allow data to be written to or read from the storage nodes Q and Qb [11]. During the read operation, the two bit-lines are pre-charged and when WL is enabled, one of the bit-lines will discharge through the access transistor and pull-down transistor depending on the stored logic levels. Although two bit-lines are not required, they are frequently used to increase noise margins by providing both the signal and its inverse [17].

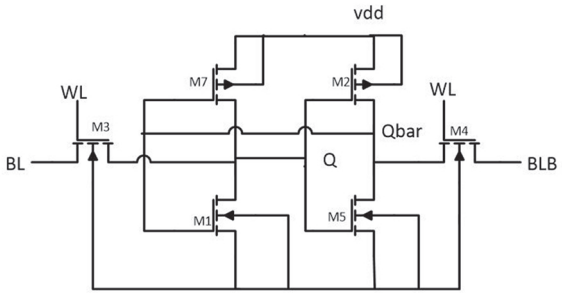


Fig. 1. Conventional 6T SRAM cell

The 6T SRAM circuit is the most area-efficient with a symmetrical layout compared to other SRAM designs [18]. However, the circuit requires pre-charging of the bit-lines and does not have separate write and read ports, thus, being unable to write and read simultaneously. For reliable operations, a certain cell-ratio (CR) and pull-up ratio (PR) needs to be maintained [19]. Process variation and supply scaling make the 6T architecture inefficient in the subthreshold region [20].

The 8T SRAM cell addresses several constraints of the 6T circuit including a separate read port, as shown in Fig. 2 [12]. The write operation is identical to that of the 6T circuit where the write word-line (WWL) is charged to turn on the access transistors and data is applied in the bit-lines. Data is stored in the nodes Q and Qb. During read operation, WWL is set to zero voltage and read bit-line (RBL) is pre-charged. When read word-line (RWL) is charged, RBL will discharge through M7 and M8 if '0' is stored in Q ('1' in Qb). When logic '1' is stored in Q ('0' in Qb), the RBL will not discharge and remain at high logic. Although the write signal can be applied in this circuit during read function, the RBL will need to be recharged before the next read operation.

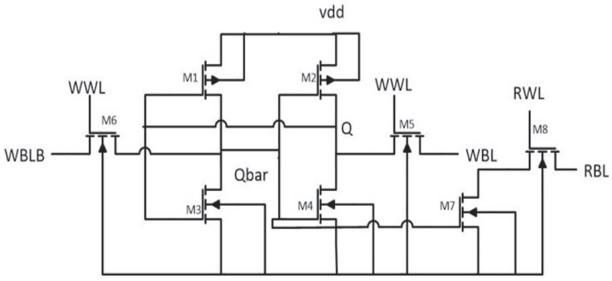


Fig. 2. 8T SRAM cell

The architecture of 9T SRAM cell consists of the 6T write cell with 3 additional transistors for the read circuit, as shown in Fig. 3 [13]. Write operation is identical to that of the 6T circuit. For the read operation, the bit-lines need to be pre-charged just like in the 6T SRAM cell. However, this time the discharging of the bit-lines occur through M7 or M8 (depending on the stored data of Q and Qb), and M9. The read-line (RL) signal enables the read circuit and if '1' is stored in Q, the BL is discharged through M7 and M9, while BLB remains at a high state. Since the storage nodes are isolated from the read path, the 9T SRAM cell provides an improved read static noise margin (RSNM) from the 6T SRAM cell.

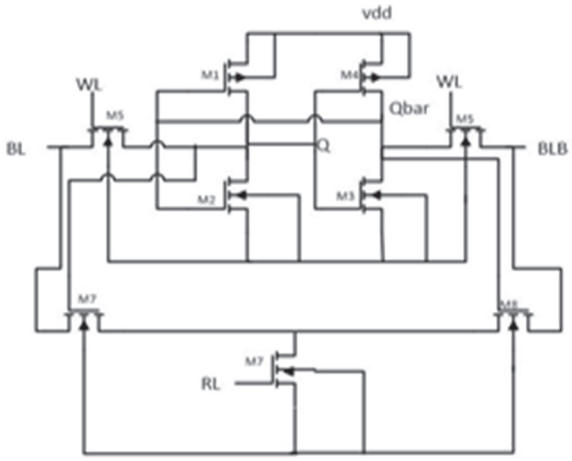


Fig. 3. 9T SRAM cell

Figure 4 shows a 10T SRAM cell presented in [14]. During the read operation, WL is charged while WWL remains at logic low, disabling transistors M3 and M4. Therefore, the storage nodes are isolated from the read path which improves the RSNM. The node VG (virtual ground) is set to 0 V. The bit-lines are pre-charged and if '1' is stored in Q, then BL discharges through M8 and M9 while BLB remains at a high state. On the other hand, if '0' is stored in Q i.e. '1' stored in Qb, then BLB discharges through M6 and M10 while BL remains at the pre-charged value. The read operation is thus enabled by charging WL. During the write operation, both WL and WWL are charged, and VG is also

set to logic high voltage to disable the discharging path. The data from the bit-lines are, thus, stored at the storage nodes. However, since the write operation now includes two access transistors, the write delay is higher compared to other SRAM circuits.

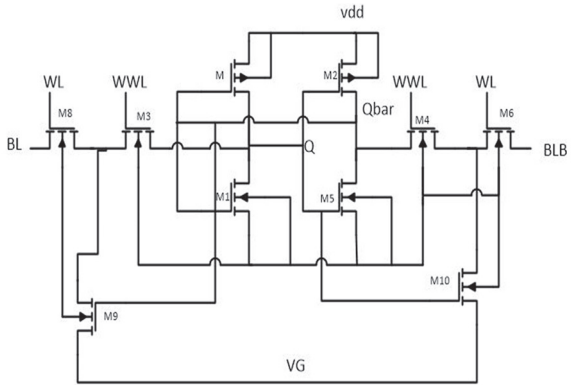


Fig. 4. 10T SRAM cell

3. PROPOSED DESIGN

The proposed 8T SRAM cell is shown in Fig. 5, which consists of a 5T write cell (M1-M5) and a 3T read cell (M6-M8). The write cell includes two cross-coupled CMOS inverters and an access transistor M3 which is enabled by the write-line (WL). Data is applied only through one bit-line and stored in the nodes Q and Qbar. The read cell consists of a single CMOS inverter and an access transistor M6 which is enabled by the read-line (RL). The CMOS inverter is connected between read-bit-line (RBL) and ground where RBL is charged during the read operation. Data is read from the node R/O. The access transistors M3 and M6 operate during write and read operations, respectively. A detailed operation of the SRAM cell is given below.

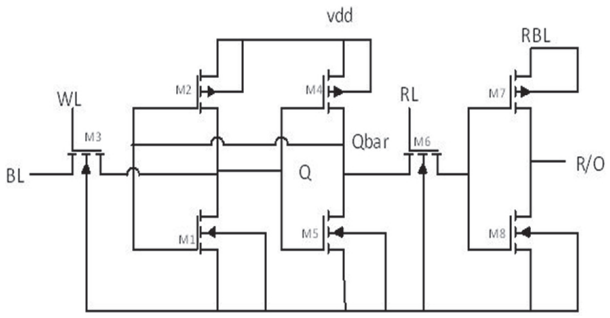


Fig. 5. Proposed 8T SRAM cell

Write '0': Write-line (WL) is charged and logic '0' is applied at BL. The data from BL is transferred through M3 to the storage node Q. The node Q is also connected to the gate of M4 which is turned on to pull-up Qbar to the supply voltage Vdd. As a result, logic '1' is stored in Qbar. This turns on the transistor M1 to connect node Q to the ground and, therefore, write '0'.

Write '1': Write-line (WL) is charged and logic '1' is applied at BL. The data from BL is transferred through M3 to the storage node Q. This high logic turns on M5 to connect Qbar to the ground and store '0'. Logic '0' in node Qbar turns on M2 to connect Q to the supply voltage Vdd. After WL is disabled, the two storage nodes are latched and '1' is stored in node Q.

Read '0': During read operation, RBL is set to logic high voltage. When Q stores logic '0', '1' is stored in Qbar. After RL is charged, data '1' from Qbar is accessed which enables transistor M8 and the R/O is connected to the ground and '0' is read.

Read '1': When '1' is stored in Q, '0' is stored in Qbar. After RL is charged, logic '0' from Qbar is transferred through M6 to turn on M7 and connect R/O to RBL. Since RBL is set to logic high, '1' is read at the output.

Unlike the reported SRAM cells in literature, the proposed design circumvents the need of any pre-charging step during the read operation. The read circuit is completely isolated from the write circuit, thus, allowing simultaneous and parallel read and write operations. After RBL is charged, the read circuit is enabled and data can be read by charging RL. If RL is set to '0' and RBL remains at '1', previous data is read from the cell. During this scenario, new data can be written in parallel to the read function in the cell by charging WL while R/O keeps showing the previously stored data. Additionally, real-time data can be read simultaneously as it is being written if both RL and RBL remain at '1' during the write operation. However, when RBL is disabled, the output from R/O is invalid regardless of the state of RL. Furthermore, the isolation of the read path from storage nodes improves the read operation stability.

4. RESULTS

LTspice platform is used to simulate proposed and current SRAM cells in predictive technology model (PTM) 16 nm technology. Read and write latency, read and write power consumptions, PDP, and noise margin are evaluated to assess the performance of the topologies. The supply voltage was 0.9 V.

Figure 6 presents the transient operation of the proposed SRAM cell during write hold operations. With precise voltage levels, both '0' and '1' data were written successfully. Additionally, data is successfully overwritten without any distortions.

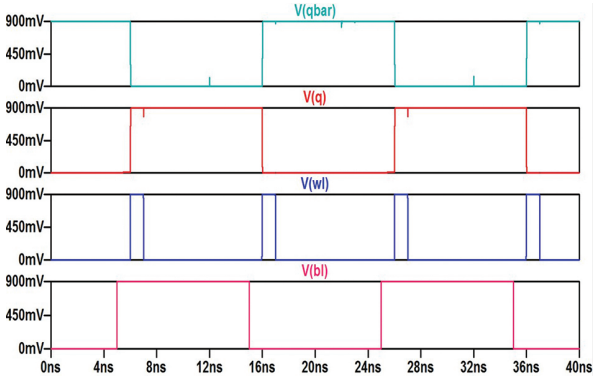
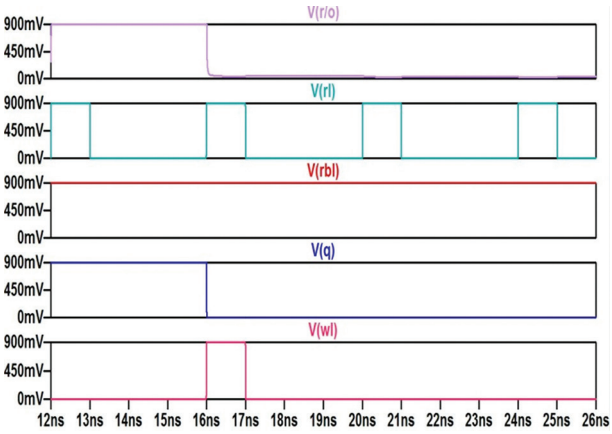
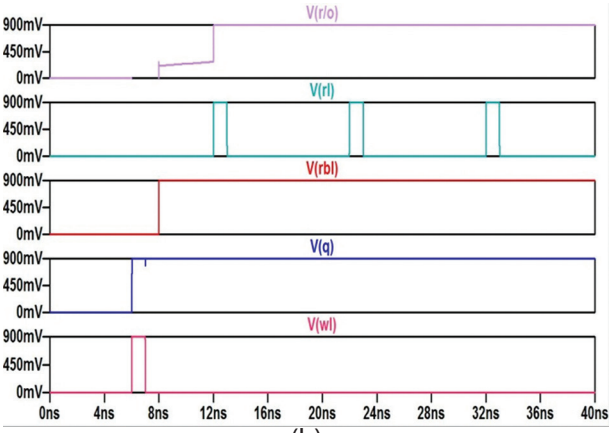


Fig. 6. Write operation of proposed 8T SRAM cell

It is considerably more difficult to read data in the existing SRAM architectures than to write it. The read data disappears once the read cycle is through. The circuit needs to be reset to read the data again. However, successive read operations can be easily performed by simply charging RL repeatedly. The voltage at R/O stays constant throughout subsequent read operations, which is evident from Fig. 7. Repetitive read operations do not add any initialization or propagation delay. RBL can be maintained at a logic low when a read operation is not required, which lowers the circuit's power requirement.



(a)



(b)

Fig. 7. (a) Successive read '0', and (b) successive read '1' operations of proposed 8T SRAM

Simultaneous read and write operations in the proposed SRAM cell are shown in Fig. 8. Once RL and RBL are charged to logic high, the read circuit is enabled and data is read at R/O. When WL is enabled to write data, R/O changes with the storage node Q, and data is read simultaneously as it is written. The write action is unaffected by the read operation.

Fig. 9 shows the comparison of write '0' and write '1' delay for all the studied SRAM cells at a supply voltage of 0.9 V. The proposed 8T SRAM cell has lower write '0' latency than all the other SRAM cells and lowers write '1' delay compared to 8T and 10T SRAM cells. Fig. 10 shows the comparison of the read '0' and read '1' delay for all the studied SRAM cells. The read operation for the existing circuits with pre-charging is performed by adding a 1 fF capacitor. Based on the results, the proposed design significantly improves the read delay.

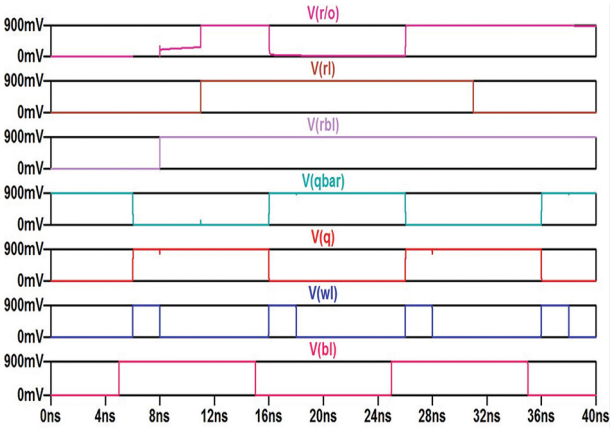


Fig. 8. Simultaneous Read-write operations of proposed 8T SRAM

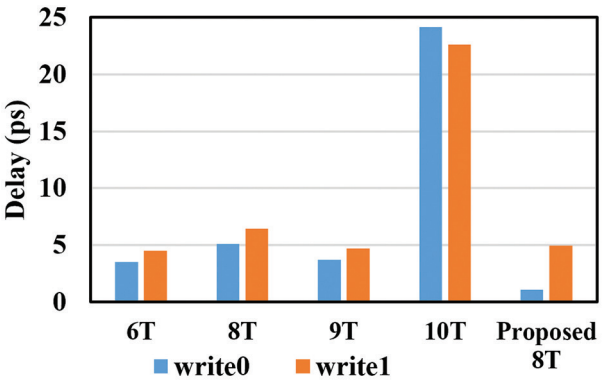


Fig. 9. Calculated write delay comparison

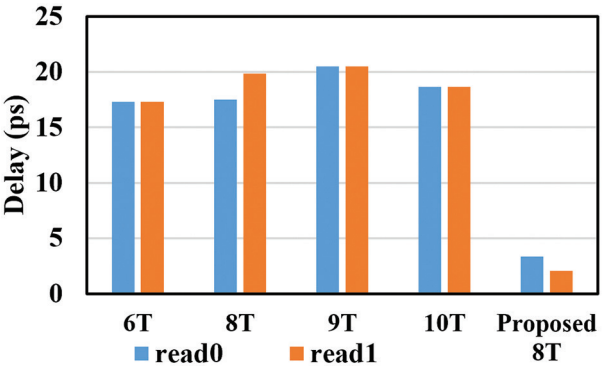


Fig. 10. Calculated read delay comparison

Table 1. Comparison of write and read power of different SRAM cells

Cell	Power (uW)			
	Write 0	Write 1	Read 0	Read 1
6T	12.56	12.56	0.93	0.92
8T	11.75	11.05	0.22	0.34
9T	13.06	12.70	1.40	1.40
10T	13.53	13.53	0.22	0.22
Proposed 8T	18.09	5.19	0.99	0.52

The write and read power consumptions of the investigated cells are compared in Table 1. Results show that the proposed 8T SRAM cell has a lower power penalty for write '1' operation compared to previously reported topologies, but a higher write '0' and comparable read power penalties. The increased power consumption during write '0' is due to the absence of the complementary bit-line and voltage drop across the single access transistor when passing logic '0'.

Fig. 11 presents the comparison of PDP of different SRAM topologies. Our proposed 8T SRAM cell has the lowest write '1' PDP compared to other architectures. For read '1' operation the proposed cell has the lowest PDP, while read '0' PDP is significantly lower compared to that of 6T and 9T cells.

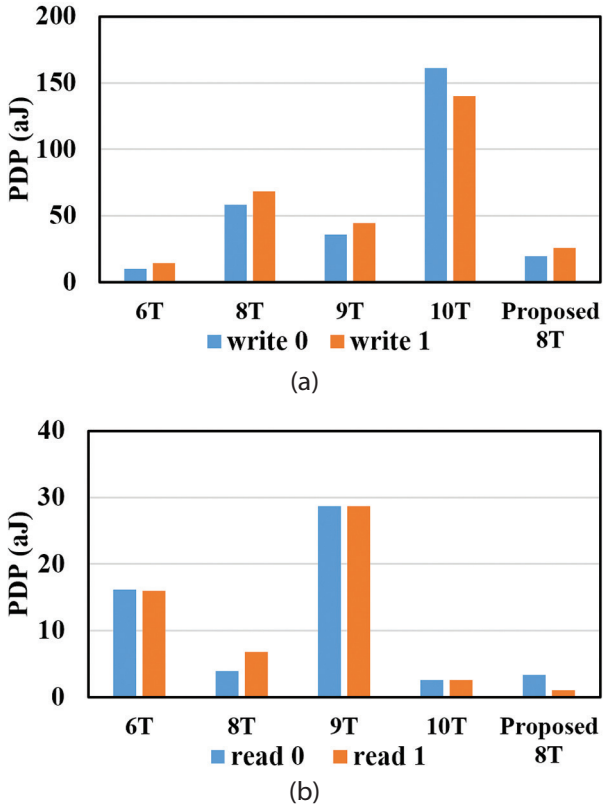


Fig. 11. PDP of (a) write, and (b) read operations of different SRAM topologies.

The noise margin of the proposed cell is compared with existing 6T, 8T and 9T topologies in Fig. 12. Results show that the proposed read circuit provides an improved read noise margin compared to 6T and 9T cells. Moreover, the proposed cell has the largest write '0' noise margin.

Since different SRAM topologies may perform superior to others in terms of different parameters, it is necessary to compare them in terms of a single numerical quantity that considers all other characteristics to evaluate the efficiency. This parameter is called the figure of merit (FoM) and is defined by Equation (1), where a larger value indicates better performance. Table 2 compares the FoM of different topologies and the results show that the proposed SRAM cell is the most efficient with the highest value.

$$FoM = \frac{sum\ of\ Noise\ Margins}{sum\ of\ PDPs}$$

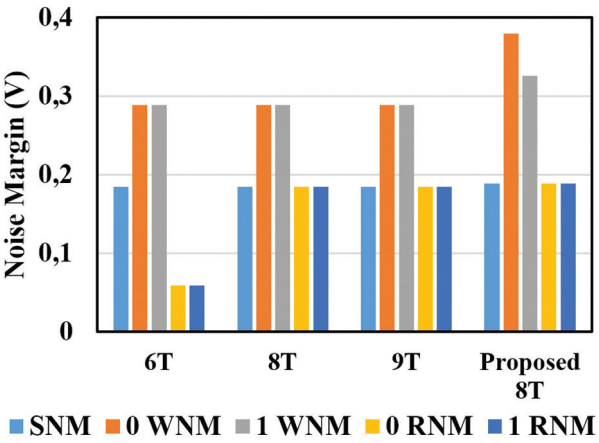


Fig. 12. Comparison of Noise Margin of Proposed cell with the other SRAM topologies.

Table 2. FoM comparison of different SRAM cellsa

Cell	FoM
6T	15.50
8T	8.24
9T	8.23
Proposed 8T	25.60

The proposed cell is also simulated using the 10nm Berkeley Short-channel IGFET Model-Common Multi-Gate (BSIM-CMG) FinFET model to investigate the robustness of the circuit at a different technology node. The performance is compared with the conventional 6T SRAM cell. Tables 3, 4, and 5 present the comparisons for delay, power, and PDP, respectively. The proposed cell has a lower read and write delay. Although power consumption is higher, the PDP is significantly lower for write and read '0' and read '1'.

Table 3. Comparison of write and read delay of different SRAM cells at 10nm node

Cell	Delay (ps)			
	Write 0	Write 1	Read 0	Read 1
6T	2.99	3.99	22.8	22.8
Proposed 8T	0.58	1.26	3.64	1.84

Table 4. Comparison of write and read power of different SRAM cells at 10nm node

Cell	Power (uW)			
	Write 0	Write 1	Read 0	Read 1
6T	9.48	9.48	0.10	0.10
Proposed 8T	13.8	0.60	1.6	0.94

Table 5. Comparison of write and read PDP of different SRAM cells at 10nm node

Cell	PDP (aJ)			
	Write 0	Write 1	Read 0	Read 1
6T	28.35	37.83	2.30	2.30
Proposed 8T	8.00	0.75	5.82	1.72

5. CONCLUSIONS

This study compares a modified SRAM cell with 8 transistors to previously reported standard cells, such as 6T, 8T, 9T, and 10T. Making reading operations more effective and simple is the aim of this study. The recommended SRAM cell separates the read and write operations and does away with the necessity for bit line precharging. As a result, it is simple and reliable to carry out simultaneous read and write operations. The read 0 delay is reduced by 80.70%, 80.91%, 83.70%, and 82.07% when compared to 6T, 8T, 9T, and 10T cells, respectively. Meanwhile, read 1 latency is reduced by 88.16 percent, 89.68 percent, 90 percent, and 89 percent, respectively, in comparison to 6T, 8T, 9T, and 10T cells, in addition to enhanced noise margin and low PDP. However, the difference in delay for read '0' and read '1' indicates unsymmetrical operation which may be improved along with power consumption in future work.

6. REFERENCES

[1] Y. He, J. Zhang, X. Wu, X. Si, S. Zhen, B. Zhang, "A half-select disturb-free 11T SRAM cell with built-in write/read-assist scheme for ultralow-voltage operations", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 27, No. 10, 2019, pp. 2344–2353.

[2] S. Gupta, K. Gupta, N. Pandey, "Pentavariate Vmin analysis of a subthreshold 10T SRAM bit cell with variation tolerant write and divided bit-line read", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 65, No. 10, 2018, pp. 3326–3337.

[3] A. Agal, Pardeep, B. Krishan, "6T SRAM Cell: Design And Analysis", International Journal of Engineering Research and Applications, Vol. 4, No. 3, 2014, pp. 574–577.

[4] M. Devi, C. Madhu, N. Garg, "Design and analysis of CMOS based 6T SRAM cell at different technology nodes", Materialstoday: proceedings, Vol. 28, No. 3, 2020, pp 1695-1700.

[5] V. Sharma, F. Catthoor, W. Dehaene, "SRAM bit cell optimization," SRAM Design for Wireless Sensor Networks, Springer New York, 2013, pp. 9-30.

[6] D. Sharma, S. Birla, "Design and Analysis of 10T SRAM Cell with Stability Characterizations", Proceedings of the International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies, Bhilai, India, 19-20 February 2021.

[7] W. Lim, H. C. Chin, L. S. Cheng, M. L. P Tan, "Performance evaluation of 14nm FinFET-based 6T SRAM cell functionality for DC and transient circuit analysis", Journal of Nanomaterials, Vol. 2014, July 2014.

[8] A. Azizi-Mazreah, M. T. M. Shalmani, H. Barati, A. Barati, "Delay and energy consumption analysis of conventional SRAM", International Journal of Electrical and Computer Engineering, Vol. 2, No. 1, 2008, pp. 35-39.

[9] Y. Kumar, S. K. Kingra, "Stability analysis of 6T SRAM cell at 90nm technology", International Journal of Computer Applications, 2016, pp. 32-36.

[10] M. Yamaoka, Y. Shinozaki, N. Maeda, Y. Shimazaki, K. Kato, S. Shimada, K. Yanagisawa, K. Osada, "A 300-MHz, 25 µA /Mbitleakage on-chip SRAM module featuring process-variation immunity and low-leakage-active mode for mobile-phone application processor", IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, 2005, pp. 186-194.

[11] N. Rahman, B. Prasad Singh , "Static-Noise-Margin Analysis of Conventional 6T SRAM Cell at 45nm Technology", International Journal of Computer Applications, vol. 66, No. 20, 2013, pp. 19-23.

[12] D. Mittal, V. K. Tomar, "Performance Evaluation of 6T, 7T, 8T, and 9T SRAM cell Topologies at 90 nm Technology Node", Proceedings of the 11th International Conference on Computing, Communication and Networking Technologies, Kharagpur, India, 1-3 July 2020, pp. 1-4.

[13] C. Yu, M. Shiau, "Single-Port Five-Transistor SRAM Cell with Reduced Leakage Current in Standby", International Journal of VLSI Design & Communication Systems, Vol. 7, No. 4, 2016, pp. 1-11.

[14] G. Prasad, "Novel low power 10T SRAM cell on 90nm CMOS", Proceedings of the 2nd International Conference on Advances in Electrical, Electronics,

Information, Communication and Bio-Informatics, Chennai, India, 27-28 February 2016, pp. 109-114.

[15] J. Yang, L. Chen, "A New Loadless 4-Transistor SRAM Cell with a 0.18 µm CMOS Technology", Proceedings of the Canadian Conference on Electrical and Computer Engineering, Vancouver, BC, Canada, 22-26 April 2007, pp. 538-541.

[16] B. Majumdar, S. Basu, "Low Power Single Bitline 6T SRAM Cell With High Read Stability", Proceedings of the international Conference on Recent Trends in Information Systems, Kolkata, India, 21-23 December 2011, pp. 169-174.

[17] A. S. V. S. V. P. D. Kumar, B. S. Suman, C. A. Sarkar, D. V. Kushwaha, "Stability and Performance Analysis of Low Power 6T SRAM Cell and Memristor Based SRAM Cell using 45NM CMOS Technology", Proceedings of the International Conference on Recent Innovations in Electrical, Electronics & Communication Engineering, Bhubaneswar, India, 27-28 July 2018, pp. 2218-2222.

[18] K. Osada, Y. Saitoh, E. Ibe, K. Ishibashi, "16.7-fA/cell tunnelleakage-suppressed 16-Mb SRAM for handling cosmic-ray-induced multierrors", Proceedings of the IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 13 February 2003, pp. 302-494.

[19] H. Kumar, V. K. Tomar, "A Review on Performance Evaluation of Different Low Power SRAM Cells in Nano-Scale Era", Wireless Personal Communication, Vol. 117, 2020, pp. 1959-1984.

[20] M. U. Mohammed, A. Nizam, Liaquat Ali, M. H. Chowdhury, "FinFET based SRAMs in Sub-10nm domain", Microelectronics Journal, Vol. 114, 2021, pp. 1-14.