Harmonic reduction using Particle Swarm Optimization based SHE Modulation Technique in Asymmetrical DC-AC Converter

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Abstract *– Many inverters play an important role in transmitting and processing energy to power system networks. To reduce the cost and size of multilevel inverters, various topologies have been included in the literature. But these topologies do not look at the complete harmonic distortion in the output waveform. In this study, a modern multilevel inverter structure, a mutated H-bridge inverter is adopted that demands a small amount of switches, driver circuits, power diodes and DC voltage sources compared to conventional multilevel inverters to produce the required level in the output voltage. The mutated H-bridge converter uses a nearest-level control method, produces high value of total harmonic at the output voltage and low-level harmonics content is also high, which is more dangerous than high-order harmonics. Therefore, the selective harmonic elimination (SHE) method is used to reduce the low frequency harmonics and the total harmonic distortion to the output voltage. Comparison of complete harmonic deviation and low-level harmonic content using the above-mentioned control strategies on the 31-level inverter is presented. Simulation studies confirm the performance of a 31-level inverter with low-order harmonics and a complete harmonic distortion using the SHE process. The effectiveness and accuracy of the SHE in producing 31 level waveform is demonstrated by utilizing the test outcomes and the THD found is of the order of 2.8%, 1.7%, 1.7% and 1% for the modulation index values of 0.5590, 0.7440, and 0.8380 and 0.9110 respectively.*

Keywords*: CHB, Selective harmonic elimination technique, Asymmetric multilevel inverters, Nearest level control technique.*

1. INTRODUCTION

Multilevel converters for power conversion were first introduced in the last 30 years [1]. A common theory involves the use of a large number of DC power sources and power switches to perform power conversion. In multi-level inverters, as the number of DC power sources and power switches increases, the output waveform voltage approaches almost as a sinusoidal. Compared to a two-level inverter, the main advantages of multilevel inverters are low switching losses [2], low electrical stress on every device [3], better electronic magnetic compatibility [4] and low harmonic content in the output wave [5]. The main advantage of a multilevel inverter over traditional inverters is that it can operate at high voltage using low-voltage semiconductor switches [6], [7].

Most inverters can be divided into two categories: conventional DC sources and cascaded inverter with separate DC sources. Diode clamped inverter and flying capacitor inverter fall into the conventional category of DC sources 1], [8]. In the diode clamped inverter topology, the number of capacitors in the series is used to separate the DC bus voltage according to the step required for the output voltage waveform. But as the levels in the output voltage increases, the voltage sharing between the different capacitors becomes uneven. To overcome this problem, clamping diodes are used, but due to the use of these diodes, the cost and size of the inverter increases. In flying capacitor topology, capacitors are used as a binding device. In this topology, the voltage at every capacitor is different from that of the next capacitor. The magnitude of the volt-

age level in the output waveform depends on the differences between the voltages of the two capacitors. To produce m-levels of output voltage, m-1 capacitors are required in DC bus.

The Cascading H-bridge (CHB) inverter belongs to the second category [9], [10]. In this topology, various H-bridges with a separate DC source are connected in cascading to increase the waveform steps. This topology requires the same amount of electronic power switch as the diode clamped topology, but does not require clamping diodes. The main advantages of this topology is modularity in structure, simple control method and number of output levels can be increased or decreased by simply increasing and removing the H-bridge cell. But the formation of CHB requires a large number of power converters, DC power sources and driver circuits to produce a high level of output voltage.

Many topology having reduced number of power switches, DC power sources and driver circuits developed in [11] - [15]. In [11], asymmetric topology is presented, but the main disadvantage of this topology is the use of dual-directed switches, which increase the inverter cost. The three topology of multilevel inverter introduced in [12], are supported as diode clamped, symmetrical and asymmetrical cascaded multilevel inverter (CMLI). However the use of a transformer and rectifier on the input side to achieve a high DC voltage makes its size larger. In [13], two different algorithms are introduced in symmetric and asymmetric multilevel inverter topology. However, a high number of IGBTs were used as this topology uses dual-directed switches which are the main features of this structure.

In this study, a modern mutated H-bridge [16] is adopted to obtain an increased count of output voltage steps with a shortened number of power switch devices compared to traditional CMLI. This structure, which uses a nearest-level control (NLC) system, produces an output wave with high-magnitude harmonic content. Therefore, the selective harmonic elimination (SHE) control method is adopted to reduce or lower the harmonic content and the total harmonic distortion (THD) in the output voltage waveform. Solution for non linear equation of SHE technique describing the harmonic contents, can be solved by Resultant theory [17], Genetic Algorithm [18], theory of symmetric polynomials [19], Newton-Raphson method [20], or other appropriate means. However, as the number of levels increases, the number of polynomials in mathematics becomes so large that solving them becomes more difficult and the quality of the solution deteriorates. Therefore, the Particle swarm optimization development process is adopted in this study to calculate the shooting angle of the SHE method as it has the surface exploring power at the commencing of the run and the local exploring near the end of the run. The comparative effect of THD on the output voltage using both methods has been introduced to investigate the height of SHE efficiency. Lastly, the realization of the mutated H-bridge inverter to produce all levels of voltage using the SHE method is verified using MATLAB / SIMULINK and the experimental result of the 31-level inverter structure.

2. MUTATED H-BRIDGE INVERTER

The elemental unit in this topology is a combination of two switches and one DC voltage source with traditional H-bridge cell or it can be said that it is the combination of two DC voltage source (V_1 and $V_{1'}$) and six unidirectional power electronic switches (S_1, S_2, $S_{1'}$, $S_{2'}$, S_a and S_b) . Fig. 1 shows the elemental unit for the mutated H-bridge inverter which is able to generate 7-level in output waveform [16].

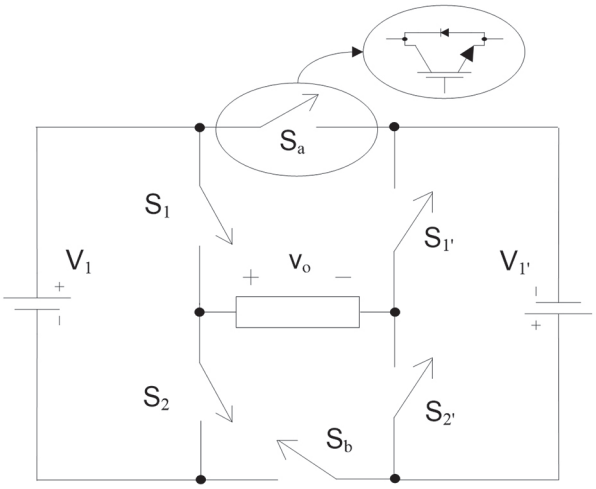


Fig. 1. Mutated H-bridge inverter structure (elemental unit) [16]

To achieve all the levels in the output waveform, the power sources V_1 and $V_{1'}$, must be in the ratio 2:1 or V_1 must be equal to the $2V_{1'}$.

The 31-level inverter structure can be upgraded using an elemental unit by connecting additional power switches and DC power sources in the manner shown in Fig. 2. This contains four DC power sources and ten different power switches. According to Fig. 2, synchronous switching (S_1, S_2), (S_3, S_4), ($S_{1'}$, $S_{2'}$) and ($S_{3'}$, $S_{4'}$) lead to shorting of DC power sources V_1, V_2, $V_{1'}$ and $V_{2'}$. Therefore, synchronous opening of these transitions must be averted. Concurrently, synchronous opening of S_a and S_a should be averted. The switch is operated as per [16] to obtain the output waveform of the multilevel inverter of the 31-level inverter.

The size of the DC voltage supplies for configuration as depicted in Fig. 2 are related by [16]:

$$V_{1'} = V_{DC} \quad (1)$$

$$V_1 = 2V_{DC} \quad (2)$$

$$V_{2'} = 5V_{DC} \quad (3)$$

$$V_2 = 10V_{DC} \quad (4)$$

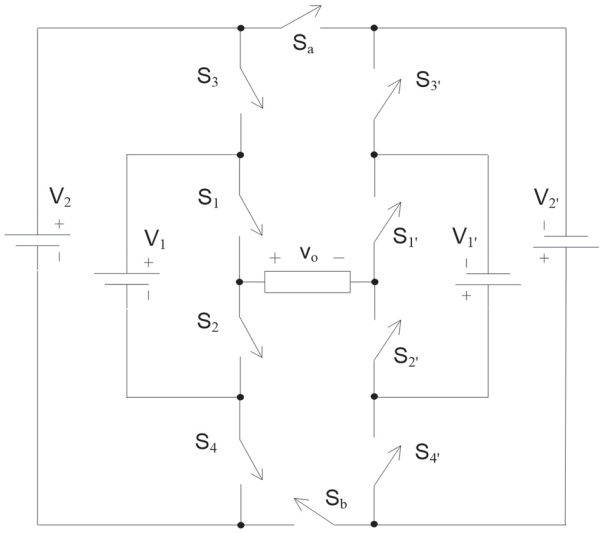


Fig. 2. 31-level inverter structure

3. MODULATION TECHNIQUES

In the literature, many variables have been introduced and can be categorized as low frequency method and high frequency method [6]. In low frequency switching methods, there is very little switching of equipment compared to high frequency methods where switching equipment is changed multiple times. The NLC, SHE, space vector control etc. comes with a low frequency change while the phase shifted, phase disposition, phase opposition disposition, space vector PWM etc. falls into the path of the most changing frequency. As the switches change frequently, switching losses increase in a highly variable mode. Therefore, the NLC and SHE strategies are adopted in this study to swap switches in a 31-level inverter structure.

3.1. NEAREST LEVEL CONTROL (NLC) TECHNIQUE

In this process [4], the reference switch signal is compared to the available voltage that can be generated and switches corresponding to that level are turned on. Here, v^* is the reference signal and the V_{aN} is the nearest available level of voltage. The output voltage can be calculated using the following equation:

$$v=V_{DC}\times round\{v^*/V_{DC}\} \quad (5)$$

Where v is the output voltage level, v^* is the reference voltage and V_{DC} is the difference between two consecutive voltage level.

A circular function is used to round the value of a variable to the nearest number [4]. Suppose, if the value of a variable is 10.7 then round it to the next value as 11 and if the value of the variable is 10.4 then round it up to the next minimum value as 10. Further details on this process can be found at [4].

3.2. SELECTIVE HARMONIC ELIMINATION TECHNIQUE

In this approach, the switching angles are predetermined in a manner to eradicate the lower magnitude of harmonics and to achieve a basic fraction equal to the reference voltage [4], [6], [21]. As an example of a seven-level inverter, the output waveform is characterized in mathematical form by extending the Fourier Series as [4], [21], [23]:

$$v_{an}(\omega t) = \sum_{k=1,3,5\ldots}^{\infty}\left(\frac{4V_{dc}}{k\pi}\right)(cos(k\alpha_1)+cos(k\alpha_2) + cos(k\alpha_3))\,sin(k\omega t) \quad (6)$$

where V_{DC} is the size of the independent DC voltage source, α_1, α_2 and α_3 are the switching angles for 1st, 2nd and 3rd unit. Switching angles to diminish the harmonics of the lower order should be calculated in such a way that $0 \le \alpha_1 < \alpha_2 < \alpha_3 \le \pi/2$. With the s number of angles, the same number of degrees of freedom is obtained, one of which is used to obtain the required output voltage and the remaining free degrees (s-1) can be used to eliminate sub-system harmonics. Using (6), the basic output voltage can be recorded by relating the switching angles as follows (assuming $k = 1$):

$$(4V_{DC}/\pi)(cos\,(\alpha_1)+cos(\alpha_2)+cos(\alpha_3)) = V_f \quad (7)$$

Magnitude of basic voltage is associated with utmost attainable output voltage by a term named modulation index m_I and can be denoted as:

$$\mathrm{m_I} = \pi \mathrm{V_f}/(4\mathrm{sV_{DC}}) \quad (8)$$

Where s is the total count of angles, V_{DC} is the DC voltage supply for every unit and V_f is the basic output voltage.

As even harmonics are absent due to the half wave symmetry of the waveform and triplen harmonics are vanished in line to line voltage. In general, the non-triplen odd harmonic components need to be eliminated or minimized. The subsequential mathematical statements are adopted to determine the switching angles:

$$\begin{aligned} \cos\,(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3) &= 3\mathrm{m}_1 \\ \cos\,(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3) &= 0 \\ cos\,(7\alpha_1)+cos(7\alpha_2)+cos(7\alpha_3) &= 0 \end{aligned} \quad (9)$$

With the given value of m_I (0 to 1), value of α_1, α_2 and α_3 are calculated by diminishing the 5th and 7th harmonic components with minimal complexity and load calculation.

To define the degree of waveform that is deviated from the appropriate sine wave, using a reference term also named total harmonic distortion (THD). It is described as the square root measure of sum of square of high frequency element to that of the basic frequency element [4], [21]:

$$THD_{49} = \frac{\sqrt{V_5^2+V_7^2+\cdots+V_{49}^2}}{V_1}\times 100 \quad (10)$$

where V_1, V_5, V_7,…,V_{49} are the magnitude of the amplitude of basic, 5th, 7th, …, 49th harmonic components

respectively. The mathematical equations as expressed in (9) are solved using the Particle Swarm Optimization (PSO) method [22].

PSO is a stochastic community conduct based on the particular and group conduct of different breed in the atmosphere in seeking of food or their requirement [22]. In this process, the particles sail in different direction in atmosphere and shift their location agreeing to their familiarity and agreeing to the surrounding particles, thus using the finest environment in which they interact with themselves and their neighbors. Every character has its current location X_i=[x_{i1} , x_{i2},…x_{iD}] and a velocity V_i= [v_{i1} ,v_{i2} ,…v_{iD}], where D is the size of the search space. Particle speed indicates a change in location from one step to another. Every character remembers its personal finest location (p_{best}) according to the finest qualification value in the search field. Global finest value (g_{best}) is the finest value obtained by one of the characters in a group. During testing, characters adjust their position and speed from their experience and previous knowledge of other characters in the group. This means that each character changes its location and speed depending on the span between its present location and pbest and the span between its present location and g_{best}. The finest location detected by ith character is recorded and represented as $P_{best,i}$=[$P_{best,i1}$, $P_{best,i2}$, …$P_{best,iD}$]. The finest location found by another character among group characters represented as G_{best} =[G_{best1} , G_{best2},…G_{bestD}] Updated speed and status of i^{th} character in d^{th} dimension using present speed and distance from $P_{best,iD}$ and $G_{best,D}$ can be given as:

$$\mathrm{v_{iD}(t+1)} = \chi[\mathrm{v_{iD}(t)} + \mathrm{c_1 r_1}\left(\mathrm{P_{best,iD}} - \mathrm{x_{iD}(t)}\right) + \mathrm{c_2 r_2}\left(\mathrm{G_{best,D}} - \mathrm{x_{iD}(t)}\right)] \quad (11)$$

$$\mathrm{x_{iD}(t+1)} = \mathrm{x_{iD}(t)} + \mathrm{v_{iD}(t+1)}\ \mathrm{i} = 1,2,\ldots \mathrm{m} \quad (12)$$

where m is the sum of characters in group, t is the sum of repetition (generation), D is the sum of dimensions corresponds to sum of members of every character, v_{iD} (t+1) is the velocity of member D of character i at repetition t+1, v_{iD} (t) is the velocity of member D of character i at repetition t, x_{iD} (t+1) is the position of member D of character i at repetition t, where c_1 and $c2$ are the cogitative and group parameters respectively, $r1$ and $r2$ are the arbitrary numbers between 0 and 1, $P_{best,iD}$ is the local finest location of member D of character i.

A new factor named constriction factor χ has been inserted to enhance the convergence attribute of PSO algorithm as:

$$\chi = \frac{2\mathrm{k}}{\left|2 - \mathrm{c} - \sqrt{\mathrm{c}^2 - 4\mathrm{c}}\right|}, \mathrm{c} = \mathrm{c_1} + \mathrm{c_2}; \mathrm{c} > 4. \quad (13)$$

The calculated switching angles should produce desired basic output voltage and be in the range of 0 to π/2. In this work, the cost function used to reduce the harmonic content in the output voltage is given as follows:

$$\mathrm{f}(\alpha_1, \alpha_2, \alpha_3, \ldots, \alpha_{15}) = \mathrm{abs}\left(\mathrm{M} - \mathrm{abs}(\mathrm{v_1})\right) + \mathrm{abs}(\mathrm{v_5}) + \mathrm{abs}(\mathrm{v_7}) + \cdots + \mathrm{abs}(\mathrm{v_{43}}) \quad (14)$$

Where M=m_I * 4sV_{DC}/π and α_1, α_2, α_3,…, α_{15} are the switching angles.

4. SIMULATION RESULTS

In this section, the performance of the above-mentioned topology is validated by simulation studies employing NLC and SHE techniques for 31-level inverter configuration as depicted in Fig. 2. For NLC technique, the utmost amplitude of reference signal plays an important role in deciding the magnitude of output basic voltage However, as the magnitude of the reference signal changes, the THD at the output voltage also changes. The effectiveness of the NLC strategy is confirmed by conducting simulation studies using the parameters V_1, V_2, $V_{1'}$ and $V_{2'}$ are 30V, 150V, 15V and 75V with R–L load having R = 45Ω and L = 55mH (as stated in [16]). The output phase voltage and the current waveform obtained using the NLC methods are shown in Fig. 3. Fourier analysis of the waveforms shown in Fig. 3 is given in Fig. 4.

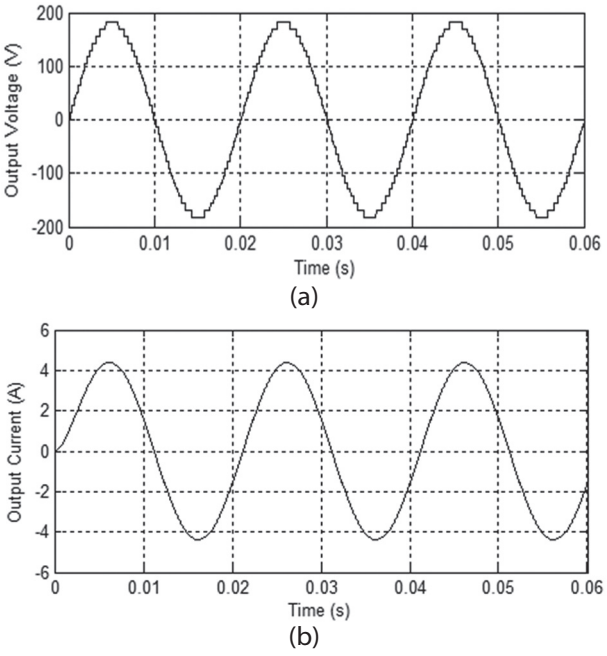
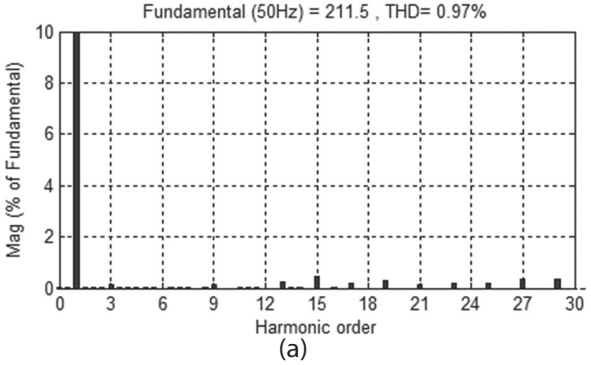
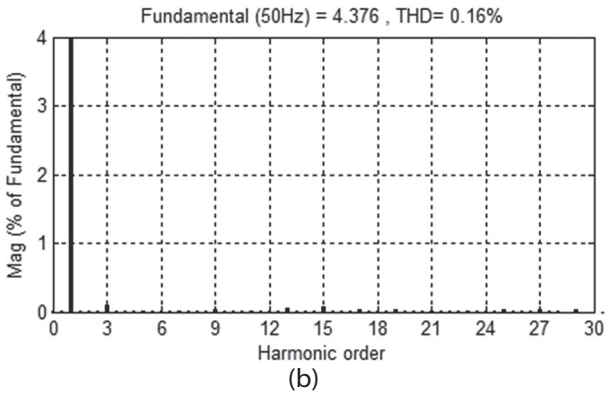


Fig. 3. Simulated waveform using NLC technique for (a) phase voltage (b) phase current.





(b)

Fig. 4. THD in output (a) phase voltage (b) phase current.

It is observed that THD values in the generated phase and current are still 0.97% and 0.16% respectively and these values are comparable to the results given in [16], i.e. 0.94% and 0.19% respectively. Therefore, the effectiveness of the NLC strategy adopted in this project is validated by simulation studies.

Using the SHE modulation scheme, the angle conversion values were obtained using the PSO method for the various modulation index values as shown in Table 1 of the 31-level inverter. For real-time use of the SHE system, changing the angles corresponding to the modulation index can be kept in the look-up table and can be changed easily and efficiently.

To ensure computerized angles using the PSO method, simulation courses in the MATLAB / SIMULINK field were developed for a 31-level converter with the following parameters: elemental frequency = 50Hz, V_1, V_2, $V_{1'}$ and $V_{2'}$ are 24V, 120V, 12V and 60V respectively (statistically (1) - (4)).

A correlation study of calculation and simulation outcomes is presented in Table 2. As shown in Table 2, for example, in m_I= 0.7440, the magnitude of the 5th and 7th harmonic components by calculation were 0.03% and 0.39% respectively while in simulation these numbers are 0.02% and 0.42% respectively. The results obtained with numeracy and simulation studies are very close. Concurrently, in some m_I values the results are very consistent. Therefore, these outcomes validate the calculation results obtained by the PSO method using simulation studies.

In order to ensure the superiority of the SHE strategy over the NLC method, simulation studies of different modulation index values were performed using the NLC method. Fig. 5 (a) shows the line voltage waveform generated using the NLC method while the corresponding waveform using the SHE method is shown in Fig. 5 (b) for m_I= 0.7440. It can be seen from these statistics that the desired levels are obtained using both methods.

Fourier analysis of line voltage obtained by NLC and SHE strategies are shown in Fig. 6 (a) and Fig. 6 (b) respectively. It can be seen from these statistics that THD values are 1.21% and 0.83% respectively in NLC and SHE's for basic output voltage of 229V.

In addition, comparative studies with respect to the lower order of harmonics shows that the magnitude of the 5th and 7th part of the waveform obtained using NLC is 0.59% and 0.43% respectively, whereas in the case of SHE these values are 0.02% and 0.42%, very small compared to the NLC method.

Table 1. Swapping angles for 31-level inverter employing SHE

Swapping angles	Modulation Index			
	0.5590	0.7440	0.8380	0.9110
α_1	25.89	2.17	0	0.26
α_2	32.68	5.46	3.27	2.86
α_3	37.96	11.90	6.43	5.86
α_4	40.45	13.79	7.07	7.62
α_5	44.89	17.87	12.86	9.93
α_6	46.15	21.81	13.27	14.25
α_7	50.85	25.76	18.37	14.57
α_8	52.89	29.50	22.86	20.10
α_9	57.10	35.51	26.82	20.92
α_{10}	61.15	41.17	31.75	26.26
α_{11}	64.38	48.86	35.48	26.28
α_{12}	67.27	53.29	39.34	32.74
α_{13}	71.99	59.75	42.33	37.53
α_{14}	76.81	67.60	50.29	41.31
α_{15}	81.22	89.98	78.96	49.05

Table 2. Correlation of calculated (C) and simulated (S) outcomes

Modulation Index	0.5590		0.7440		0.8380		0.9110	
	C	S	C	S	C	S	C	S
Fundamental r.m.s voltage (V)	171.5	171.5	226.3	229	256.4	257.4	276.2	275.9
5th Harmonic content (%)	0.05	0.19	0.03	0.02	0.07	0.08	0.13	0.26
7th Harmonic content (%)	0.06	0.15	0.39	0.42	0.11	0.20	0.16	0.12
11th Harmonic content (%)	0.03	0.05	0.04	0.11	0.03	0.04	0.01	0.09
Total Harmonic Distortion (%)	0.95	1.01	0.79	0.83	0.80	0.91	0.84	0.88

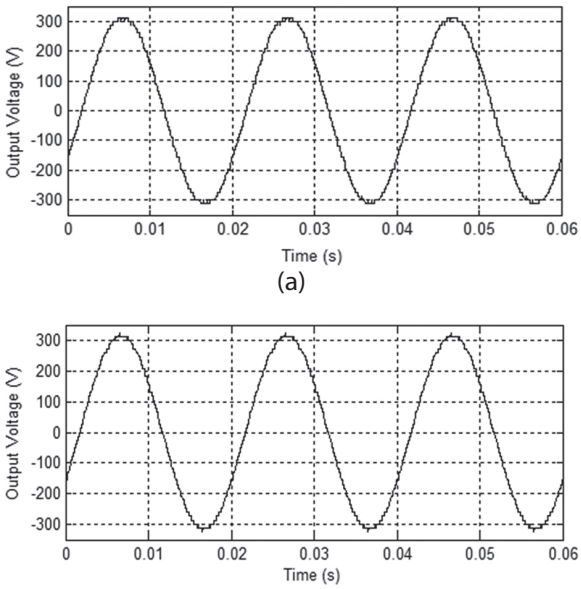


Fig. 5. Simulated waveform of output line voltage at $m_I = 0.7440$ employing (a) NLC (b) SHE.

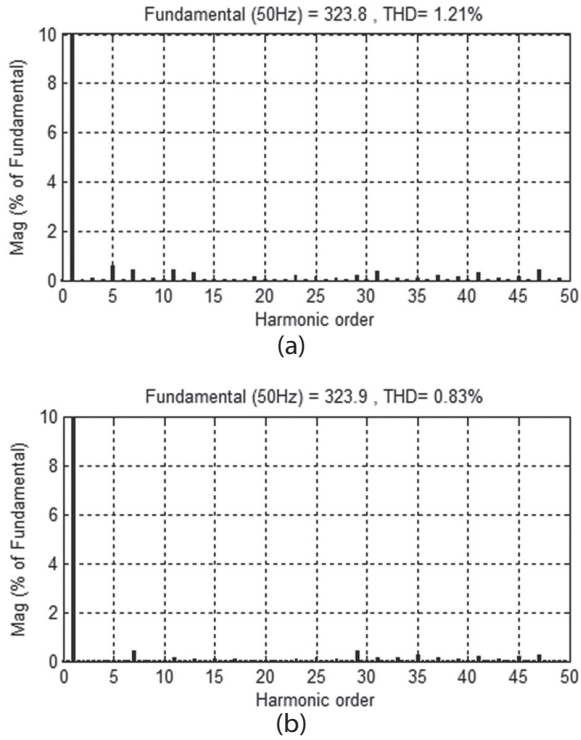


Fig. 6. Harmonic spectrum of output line voltage at m_I 0.7440 employing (a) NLC (b) SHE.

As shown in Table 3, in m_I= 0.8380, the magnitude of the 5th and 7th harmonic components using NLC is 2.63% and 1.21% respectively while using the SHE process module, 5th and 7th harmonics reduced to 0.08% and 0.20% respectively. The comparative data between the two methods is shown in Table 3.

Therefore, the above study shows that THD and the magnitude of the lower order harmonics in line voltage are much smaller in the SHE as compared to NLC. It may be noted that in the harmonic spectrum the utmost values of the basic voltage are displayed.

Table 3. Comparison of THD in output line voltage employing NLC and SHE technique

Modulation Index	0.5590		0.7440		0.8380		0.9110	
	NLC	SHE	NLC	SHE	NLC	SHE	NLC	SHE
Fundamental r.m.s voltage (V)	172.4	171.5	229	229	258.3	257.4	276.5	275.9
5th Harmonic content (%)	0.53	0.19	0.59	0.02	2.63	0.08	2.50	0.26
7th Harmonic content (%)	0.45	0.15	0.43	0.42	1.21	0.20	1.94	0.12
11th Harmonic content (%)	0.43	0.05	0.42	0.11	0.53	0.04	0.81	0.09
Total Harmonic Distortion (%)	2.07	1.01	1.21	0.83	3.03	0.91	3.33	0.88

Furthermore, in order to find out distortion in output current, a performance parameter i.e. weighted total harmonic distortion (WTHD) is calculated and defined as follow [23]:

$$WTHD_{49} = \frac{\sqrt{(V_5/5)^2+(V_7/7)^2+\cdots+(V_{49}/49)^2}}{V_1} \times 100 \quad (15)$$

Table 4. Comparison of WTHD in output line voltage

Modulation Index	NLC	SHE
0.5590	0.1522	0.0774
0.7440	0.0850	0.0588
0.8380	0.5726	0.0570
0.9110	0.5769	0.0635

The table 4 shows the comparison of WTHD in output line voltage employing the NLC and SHE technique. WTHD in case of SHE is very less as compare to NLC and comparative result in Table 4 validates the performance of multilevel inverter employing SHE technique.

5. EXPERIMENTAL RESULTS

A prototype setup is advanced in an effort to verify the diverse results received from the simulation studies as shown in Fig. 7 for 31-level inverter at m_I=0.7440. The details of numerous thing adopted for hardware implementation are as: Insulated Gate Bipolar Transistor (IGBT, FGW40N120HD) with a 1200V/40A capacity, DC voltage sources value V_1, V_2, $V_{1'}$ and $V_{2'}$ are 24V, 120V, 12V and 60V respectively. The switching pulses had been issued to

switching gadgets through dSPACE1104 and real time interfacing card. The basic output voltage of inverter may be managed in actual time via changing values of switching angles. A dead band is required to avert any short circuit due to synchronous flip-on of transfer pair (S_1, S_2) or (S_1, S_2) etc. A value of dead band relies upon the ON and OFF delay time of the electronic switch, minimum and maximum propagation delay of driver and a constant called safety margin. Considering these entire factor, a dead band of 5µsec is furnished to the switches pair. Four isolated channel digital storage oscilloscope, TPS2024B via TEKTRONIX is used for visualization of output voltage and Fluke 43B 600V/1250A is used for THD analysis in output voltage.

Fig. 7. Laboratary prototype.

A comparative study for output line voltage of 31-level inverter is carried out and has been provided in this segment. Evaluation of THD and lower order harmonic element is finished for non triplen harmonic components. Firing angles similar to numerous modulation indexes are used to operate the numerous switches. Output line voltage for 31-level inverter is shown in Fig. 8 and it could be seen that all positive and negative steps are present in the output waveform. Basic output line voltage and its THD at m_I 0.7440, 0.8380 and 0.9110 is shown in Fig. 9 (a)-(c) respectively. From Fig. 9 (a)-(c) it can be located that THD at m_I 0.7440, 0.8380 and 0.9110 is 1.7%, 1.7% and 1% respectively. A comparative result of simulation and experimental outcomes are presented in Table 5.

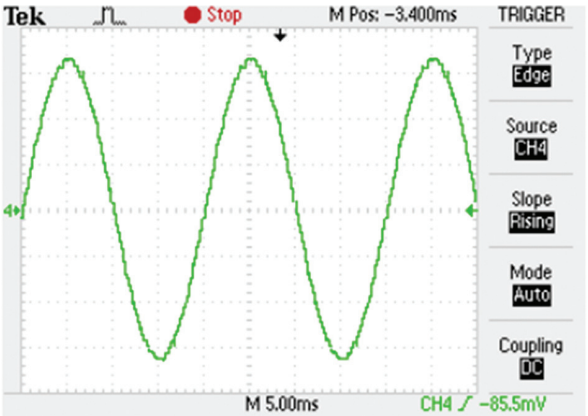


Fig. 8. Output line voltage waveform for 31-level inverter employing SHE technique at m_I= 0.7440.

A little distinction between the simulated and hardware outcomes is because of the different manner and platform adopted for these studies. Also, simulation and experimental outcomes of SHE are in near settlement and subsequently the validity of this topology with SHE technique is proved.

Table 5. Comparison of simulated (S) and experimental (E) results

Modulation Index	0.5590		0.7440		0.8380		0.9110	
	S	E	S	E	S	E	S	E
Fundamental r.m.s voltage (V)	171.5	170.3	229	225.7	257.4	254.9	275.9	276.2
5th Harmonic content (%)	0.19	0.50	0.02	0.30	0.08	0.20	0.26	0.10
7th Harmonic content (%)	0.15	0.50	0.42	0.50	0.20	0.30	0.12	0.10
11th Harmonic content (%)	0.05	0.50	0.11	0.40	0.04	0.30	0.09	0.10
Total Harmonic Distortion (%)	1.01	2.80	0.83	1.70	0.91	1.70	0.88	1.00

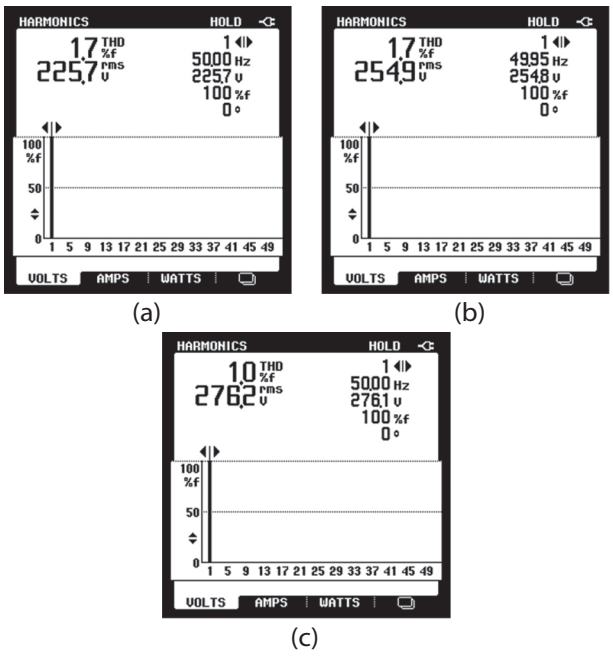
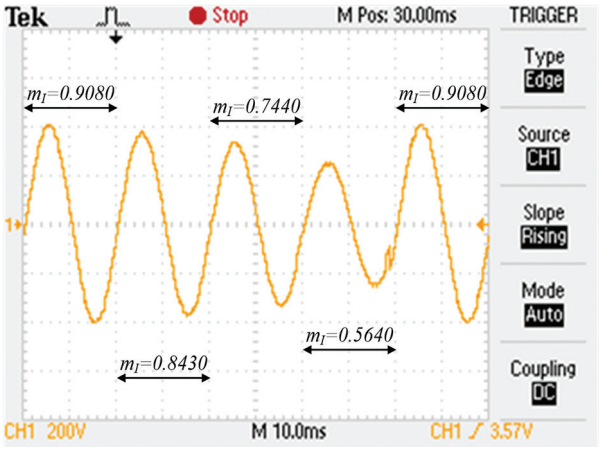


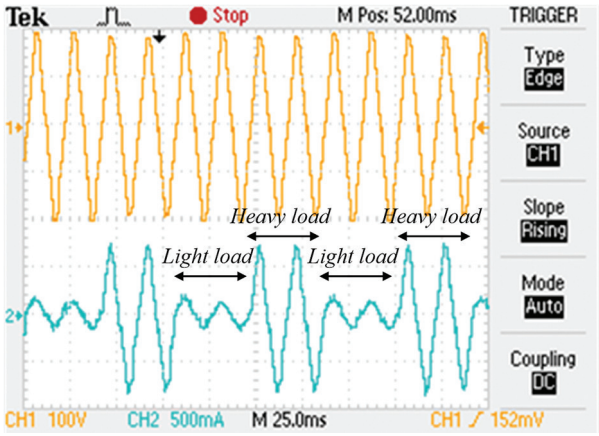
Fig. 9. 31-level output line voltage THD at m_I (a) 0.7440 (b) 0.8380 (c) 0.9110.

To analyze the dynamic behavior of this topology using the SHE method, a step change in the modulation

index and load variability is considered. The variation of the output voltage during the step change is shown in Fig. 10 (a). It is evident from this figure that there is a change in the magnitude of the output voltage (line voltage) as the m_I varies (first reduced and then increased). Load voltage and current waveforms during the change of load from light load to heavy load and from heavy load to light load are shown in Fig. 10 (b), and indicates that there is not much distortion in the output voltage waveform under the temporary condition.



(a)



(b)

Fig. 10. Output voltage waveform with (a) variation in modulation index (b) load variation.

6. CONCLUSION

In this study, a unique approach the usage of SHE method has been provided to limit the frequency component of low magnitude and total harmonic distortion in mutated H-bridge configuration. Particle swarm optimization based SHE technique is evolved for 31-level inverter. A comparative result using NLC and SHE method have been provided for 31-level inverter. The simulation and experimental results depict that proposed SHE method can diminish the lower order harmonics and THD in output voltage in comparison to NLC method. To verify the simulated consequences, experimental results are also provided. The THD found is of the order of 2.8%, 1.7%, 1.7% and 1% for the modulation index values of 0.5590, 0.7440, and 0.8380 and 0.9110 respectively using SHE for producing 31 level waveform as demonstrated by utilizing the test outcomes.This research is prospective to future studies within the subject of power conversion with high satisfactory output voltage as in renewable power where separate DC sources may be acquired by use of solar photovoltaic panel, fuel cell etc.

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