High Efficiency, Good phase linearity 0.18 µm CMOS Power Amplifier for MBAN-UWB Applications

Original Scientific Paper

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Abstract *– This paper presents the design of 3.1-10.6 GHz class AB power amplifier (PA) suitable for medical body area network (MBAN) Ultra-Wide Band (UWB) applications in TSMC 0.18 µm technology. An optimization technique to simultaneously maximize power added efficiency(PAE) and minimize group delay variation is employed. Source and Load-pull contours are used to design inter and output stage matching circuits. The post-layout simulation results indicated that the designed PA has a maximum PAE of 32 % and an output 1-dB compression of 11 dBm at 4 GHz. In addition, a small group delay variation of ± 50 ps was realized over the whole required frequency band . Moreover, the proposed PA has small signal power gain (S21) of 12.5 dB with ripple less than 1.5 dB over the frequency range between 3.1 GHz to 10.6 GHz, while consuming 36 mW.*

Keywords *– Group Delay (GD); Medical Body Area Network (MBAN); Ultra-Wide Band (UWB); Power Added Efficiency (PAE); Class AB, Power Amplifier (PA)*

1. INTRODUCTION

Tremendous development in healthcare electronics system based on the Radio Frequency (RF) CMOS technology has a great impact in the industry of bio-medical to enhance the diagnosis and health monitoring. Medical body area network (MBAN) can be defined as a wireless network consisting of small intelligent devices that can be attached to the human body surface or implanted inside the body that act as MBAN nodes for remote sensing and diagnosis [1]. The Federal Communications Commission (FCC) defined the ultra-wide band signal as the signal whose bandwidth is more than five hundred megahertz or fractional bandwidth bigger than 20% and specified the spectrum from 3.1 to 10.6 GHz for UWB applications [2]. High data rate transmission of UWB systems qualifies them to be a promising candidate for MBAN applications in real time monitoring of multi-node systems [3]. In 2012, the IEEE LAN/MAN standards committee released the IEEE 802.15.6 standard that explains the detailing of different Physical (PHY) layers for Ultra-Wideband (UWB) and Human Body Communications (HBC) layers for MBAN [4]. The objective of this standard was to develop a short-range wireless communication system for low power devices positioned around, or implanted inside the human body [3]. In this standard, As seen in Fig. 1, the 3.1 -10.6 GHz spectrum is divided into low band of three channels (channels 0-2) and high band of eight channel (channels 3–10). Each channel has a bandwidth of 499.2 MHz to achieve data rates for transmissions up to 480 Mb/s [4].

Some issues for CMOS technology such as [5] substrate coupling, poor quality factor of the on-chip passives, hot carrier effect and small oxide breakdown voltage of CMOS make the design of CMOS UWB power amplifiers a difficult and challenging task. It is required for the UWB PAs to have broadband matching, flat gain over the desired bandwidth, good linearity, small group delay, and acceptable PAE. The CMOS UWB-PAs presented in literature adopt different topologies and operate over different bands such as 3.0 to 5.0 GHz, and 6.0 GHz to 10.0 GHz [6] – [25].

The resistive shunt feedback topology [6]-[8] achieves wideband matching and better gain flatness over wide bandwidth, but suffers from its small PAE and consumes large DC power consumption. Also, the distributed amplifiers provide a good wideband matching and broad gain-bandwidth. However, it consumes large area and dissipates high DC power that re-

duces the PAE [9]. Meanwhile, the traditional common source (CS) and cascode with inductive degeneration topology provides good gain and noise performance. However, the matching is not as good as resistive shunt feedback topology [10-12]. Whereas, the current reuse structure, compared to cascode and CS structure, offers better isolation and larger gain thanks to its higher output impedance and smaller miller capacitance [13-17]. However, its main drawback is the bad input matching.

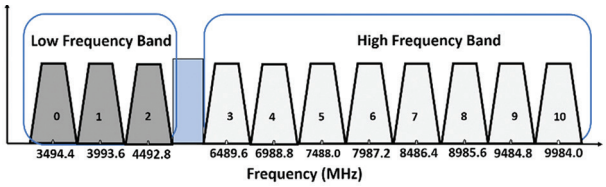


Fig. 1. UWB-MBAN operating frequency bands.

In the design of UWB systems with impulse response, it is necessary to keep the group delay (GD) constant over the whole frequency range of interest in order to avoid signal distortion. Through literature, different techniques are reported to overcome the group delay issues in the UWB PAs. The authors in [18] presented a negative group delay circuit to reduce the group delay variation in UWB InGaP/GaAs HBT MMIC amplifier. But utilizing additional negative GD circuit consumes large area and deteriorate the PAE significantly. Another technique by optimizing the value of inductors is presented in [19] but, also, it improves the GD at the expense of the reduction in PAE. Recently, David. et.al [21] improved the group delay variation using s a stacked FET structure, However, the stacked FET requires high supply voltage and should be accurately biased to avoid transistors breakdown. Generally, the PAE is important in the design of UWB-PAs as it measures the effectiveness of converting the DC power to RF output power. Therefore, a trade-off between design requirements remains existing: For example, broad bandwidth may lead to a degradation in group delay variation and PAE.

In this paper, a minimum group delay variation, well matched CMOS PA covering the frequency range from 3.1 GHz to 10.6 GHz, with a high PAE for a MBAN-UWB transmitter is designed and simulated using 0.18 µm CMOS Technology. The proposed design consists of two stages; the first diver stage is a common gate (CG) amplifier loaded with a diode connected transistor in series with a small inductor for gain maximization, and the second power stage is designed to maximize the PAE using a simple CS amplifier with series and shunt peaking inductive load to enlarge the operating bandwidth.

The remainder of this paper is organized as follows: the UWB designed PA circuit is described in section two. Section three discusses the methodology for improving the power added efficiency and group delay performance. Post layout simulation results and comparison to recently published PAs are reported in section four. Finally, the conclusion of this paper is presented in section five.

2. TWO-STAGE PA SCHEMATIC DESCRIPTION

Fig. 2(a) and (b) show the schematic and the small signal equivalent circuit of the designed UWB PA. The proposed wideband PA made up of two stages, the first stage consists of common gate (CG) driver stage while the second stage is a common source (CS) power stage with degeneration inductor Ls3 to further improve the linearity.

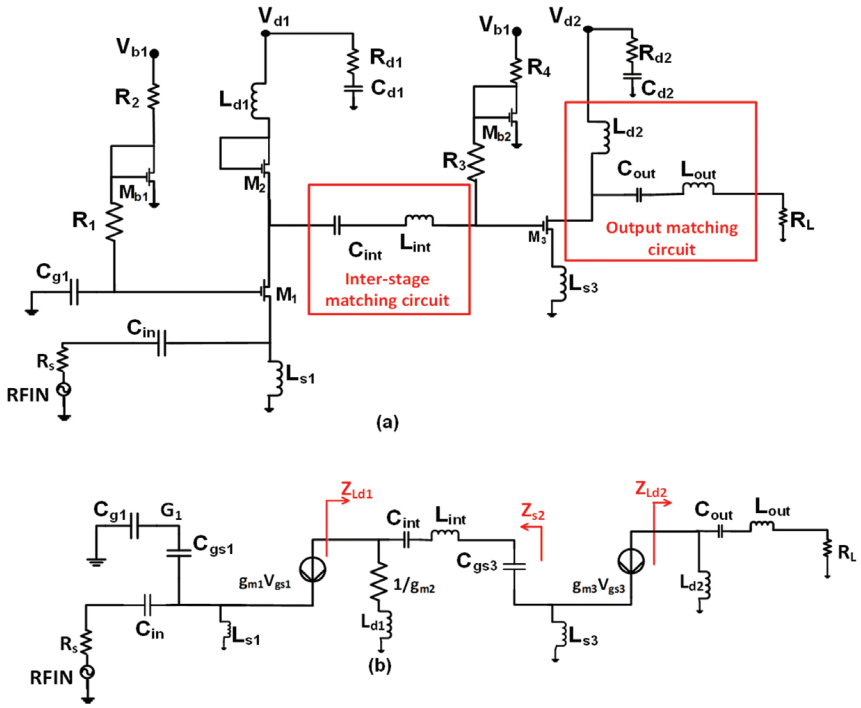


Fig. 2. (a)Circuit schematic of the designed PA (b) Small-signal equivalent circuit the designed PA.

The proposed PA is initially targeted to consume 36 mW from 2 V supply, which needs drain current of 18 mA to be divided between the two stages. *The* M_{b1}, R_1, R_2, M_{b2}, R_3 and R_4 form current mirrors that adjust the bias for transistors M_1 and M_3. The CG driver stage provides superior broadband input matching and Eq.1 expresses the input impedance of the proposed PA:

$$Z_{in} = \frac{sL_{s1}}{1 + sL_{s1}(g_{m1} + sC_{gs1})} \quad (1)$$

where g_{m1} is the transconductance of the input transistor M_1. Source inductor L_{s1} and the size of transistor M_1 are optimized to cancel the imaginary part of Eq.1 leaving the 50-ohm real input impedance [26]-[28]. In addition, compared to the CS configuration, the CG provides better isolation as there is no miller capacitance at the input and better noise performance as the gate is bypassed to ground leading to the absence of the gate noise current. To maximize the gain of the first stage, a large inductive load is required at the drain of transistor M_2. However, this large inductor will have small resonance frequency that will affect the gain flatness largely. Therefore, a diode connected transistor M_2 in series with a small drain inductor L_{d1} are utilized acting as the inductive load of the first stage which will save the area and improve the linearity while achieving reasonable flattened gain over the whole band. Fig.3 compares the effect of employing large load inductor alone or using the diode connected load in series with small load inductor on the gain flatness which indicates the enhancement of the 3-dB bandwidth by using the diode connected load.

The amplified signal from the common gate transistor M_1 is moved toward the second stage using the interstage matching composed of MIM capacitor C_{int}, large inductor L_{int} and the gate to source parasitic capacitance C_{gs3}. The Inter-stage matching is important to enhance gain flatness and at the same time affects the group delay and PAE greatly as will be discussed in section 3.

The 2nd stage consists of a CS amplifier which is designed to be biased for operation in class AB to trade-off efficiency and linearity. Fig. 4 shows the I-V wave forms of M_3 at 7 GHz with -5 dBm input power indicating class AB operation. The L_{d2} and L_{out} are exploited as a shunt and series peaking load for the second stage to realize wide flattened gain, little group delay variation and high PAE.

To realize the wide and flat gain response across the 3.1- 10.6 GHz band, a staggered tuning technique is utilized concurrently with better optimization of the value of the interstage inductor L_{int} to move away the tuning center frequency of each stage by a value related to its 3-dB bandwidth [25]. The tuning frequency can be defined by optimizing the sizes of transistors M_1 and M_3 which control to the current-gain cut-off frequencies $\omega_T = g_m/C_{gs}$, where, g_m and C_{gs} are the transconductance and gate-source capacitance, respectively. The size of the common source transistor M_3 of the second stage should be maximized to enhance the output power and power added efficiency. Therefore, only the size of M_1 and the value of the interstage inductor L_{int} are optimized to increase the gain- bandwidth. Fig.5 shows the effect of varying the interstage inductor L_{int} and the size of transistor M_1 on realizing wide and flat power gain.

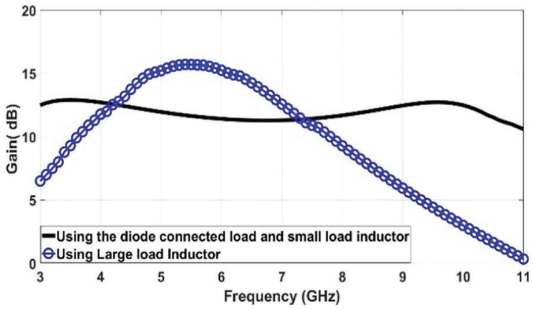


Fig. 3. Effect of employing large load inductor alone or using the diode connected load in series with small load inductor on the gain flatness.

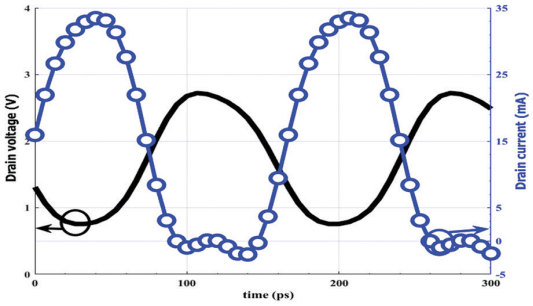


Fig. 4. The current and voltage behavior at 7 GHz for class AB PA at -5 dBm input power.

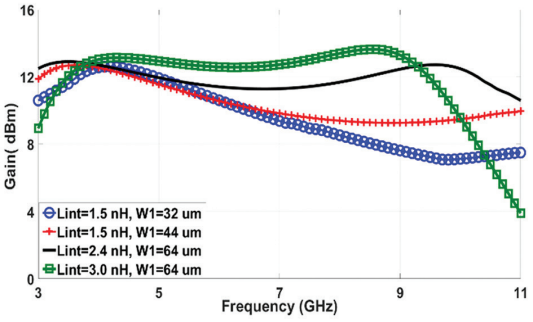


Fig. 5. Influence of changing the value of L_{int} and width of M_1 on realizing wide and flat gain.

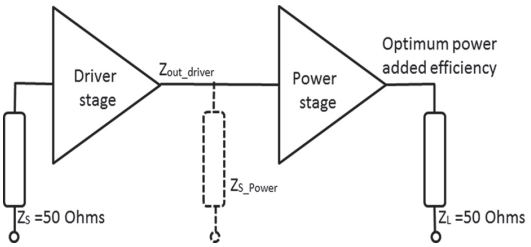


Fig. 6. Two stage power amplifiers.

3. DESIGN ANALYSIS

3.1. SOURCE AND LOAD PULL ANALYSIS

In the two-stages amplifier design as shown in Fig. 6, the output impedance of the driver amplifier (Zout_driver) is the source impedance (Zs_power) seen by the power stage. For studying the result of changing the source impedance of the second stage on the PAE, constant PAE contours are drawn in the Smith Chart, with changing source impedance using the Advanced Design System (ADS). The input signal level is fixed at -5 dBm for operation in the linear region and the load impedance is set to 50 ohms, while the impedance of the source was being changed. The constant power added efficiency contours at 4 and 8 GHz for various source impedances are shown at Fig. 7(a). As presented in Fig. 7(a), the source impedance that realize maximum PAE is existed in the inductive area of the Smith Chart. Therefore, an inter-stage matching circuit created by inductor L_{int} and capacitor $C_{int.}$ is designed and optimized to make the output impedance of the driver stage to agree with the points of maximum power added efficiency in source-pull contours of the power stage shown in Fig.7(a). Using the small signal equivalent circuit at Fig. 2(b), the output impedance of the first stage can be expressed by Eq.2:

$$Z_{out1}(s) = Z_{s2} = \frac{s^2(L_{int}+L_{d1})C_{int}g_{m2} + SC_{int} + g_{m2}}{SC_{int}g_{m2}} \quad (2)$$

As Inductor L_{int} has a fundamental role in the design of interstage matching circuit, it is optimized for maximizing the PAE, in addition to, taking into consideration gain flatness, group delay variation, chip size and input / output impedance matching.

Using the load-pull simulation in ADS and following similar steps, we can search for the optimum load location on Smith Chart which maximizes the PAE over the whole band. Fig. 7(b) reports the constant PAE contours on Smith Chart at 4, and 8 GHz using various load impedances for the second stage PA while the source impedance is fixed with the optimum impedance from the source-pull simulation.

The load impedance of the designed PA after adding the output matching can be written as:

$$Z_{Ld2}(s) = sL_{d2} \,\|\, \left(\frac{s^2L_{out}C_{out}+1}{sC_{out}} + R_L\right) \quad (3)$$

The output matching circuit is made up of the series peaking inductor L_{out} and shunt peaking inductor L_{d2} to match the load impedance Z_{ld2} with the load-pull contours at Fig.7(b) for maximum PAE.

Based on the prior description, L_{int}, L_{out} and L_{d2} affects the PAE significantly. Hence Fig. 8 presents the Influence of changing their values on realizing high PAE.

3.2. GROUP DELAY

Group delay (GD) is utilized as an effective test for signal distortion and can be calculated by taking the derivative transfer function phase with respect to angular frequency. A simplified formula for the overall transfer function H(s) and group delay can be expressed by Eq.4, Eq.5 and Eq.6.

$$H(s) = |H(j\omega)|e^{j\theta(\omega)} = -\frac{g_{m1}g_{m3}SL_{eq}(1 + Sg_{m2}L_{d1})}{S^2C_{eq}g_{m2}(L_{int}+L_{d1}) + SC_{eq} + g_{m2}} \quad (4)$$

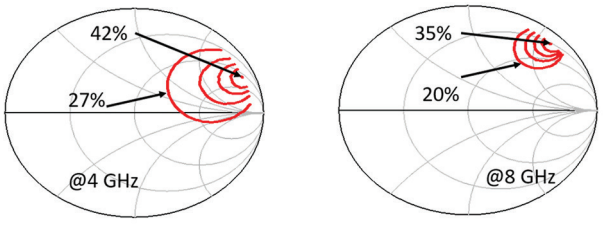
Where $C_{eq} = \frac{C_{\text{int}}C_{gs3}}{C_{\text{int}}+C_{gs3}}$ and $L_{eq} = \frac{L_{\text{d2}}L_{\text{ser}}}{L_{\text{d2}}+L_{\text{ser}}}$

$$G_D(\omega) = -\frac{\partial(\theta(\omega))}{\partial\omega} \quad (5)$$

After simplification and guided by ref [16];

$$G_D(\omega) \simeq -\frac{L_{int} + \frac{1}{\omega^2C_{gs3}}}{\frac{(1+Sg_{m2}L_{d1})}{g_{m2}} + \frac{g_{m2}}{(1+Sg_{m2}L_{d1})}\left(L_{int}\omega - \frac{1}{\omega C_{gs3}}\right)^2} \quad (6)$$

Based on the derived formula of the GD presented in Eq.6 and circuit simulation at Fig.9, Inductor L_{int} has a great effect on the GD variation where increasing its value will improve the GD performance. However, larger value of L_{int} will reduce the 3-dB bandwidth largely as concluded from Fig.5. Therefore, according to the previous explanation and guided by Fig. 5, 8, and 9, Inductors L_{int}, L_{out} and L_{d2}, in addition to the sizes of transistor M_1 and M_2, have large effect on the gain- bandwidth, PAE and group delay. For example, increasing the size of L_{int} will improve the PAE and GD variation at the expense on a reduction on the 3-dB bandwidth. Therefore, we have concurrently optimized their values to improve PAE, minimize GD variations and realize wide flattened gain simultaneously. After many optimization trials, the values of L_{int}, L_{out} and L_{d2}, are optimized and selected to be 2.8 nH, 0.46 nH, and 3 nH, respectively after EM simulation is performed.



(a)

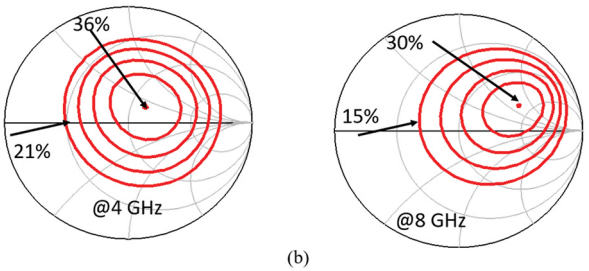


Fig. 7. (a) Constant PAE contours in 3% step at 4and 8 GHz for varying source impedance of 2nd stage. **(b)** Constant PAE contours in 3% step at 4 and 8 GHz for varying load impedance of 2nd stage.

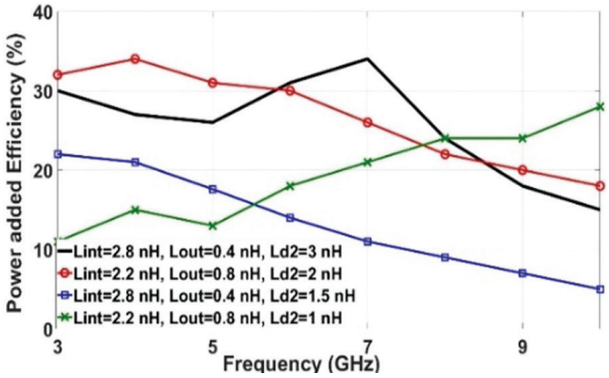


Fig. 8. Influence of changing the value of L_{int}, L_{out} and L_{d2} on the maximum PAE over the 3-10 GHz band.

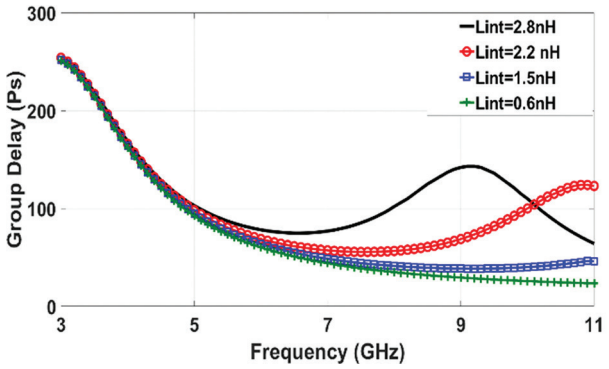


Fig. 9. Influence of changing the value of L_{int} on realizing small GD variations.

4. POST-LAYOUT SIMULATION RESULTS

The proposed UWB-PA has been designed and simulated in TSMC 0.18 µm CMOS technology. The layout of the PA is shown in Fig. 10 with size of 0.55 mm^2 including the measurement pads.

A. Pre and post layout simulated S-parameters:

Fig. 11 and Fig. 12 show the correspondence between the pre-and post-layout S-parameters using Cadence Spectre. As presented in Fig. 11, an average small signal gain($|S_{21}|$) of 12.5 ±1.5 dB and reverse isolation ($|S_{12}|$) better than -25 dB are achieved over the 3.1 to 10.6 GHz. Furthermore, a post-layout input return loss ($|S_{11}|$) and output return loss ($|S_{22}|$) less than -4.5 dB and -8.5 dB, respectively are realized also over the frequency of interest as illustrated in Fig.12.The wideband matching of the designed PA enhance the PAE and improve the GD vatiations.

B. Large Signal Simulations (Output 1dB compression point and PAE)

The harmonic balance simulation is used to test the large signal performance across the required frequency band. As shown in Fig.13 The maximum achieved PAE by the designed PA at 4 GHz, 7 GHz and 9 GHz are 32.5%, 20% and 18%, respectively. Besides that, the designed UWB-PA achieved output 1-dB compression points of, 11, 6 and 3.5 dBm and saturated output power of, 13, 11.5, and 10 dBm, at 4, 7 and 9 GHz, respectively as illustrated in Figure 14.

C. Group delay, DC power and stability:

As shown in Fig. 15, good post-layout simulated phase linearity (i.e., small group delay variation) of ±50 ps is achieved over the targeted frequency. In addition, the stability factor of the designed PA is greater than one, demonstrating that it is uncondionally stable over a wide frequency band from 0.5 GHz to 16 GHz as shown in Fig.16. In normal biasing conditions, the PA consumes 36 mW from 2 V supply.

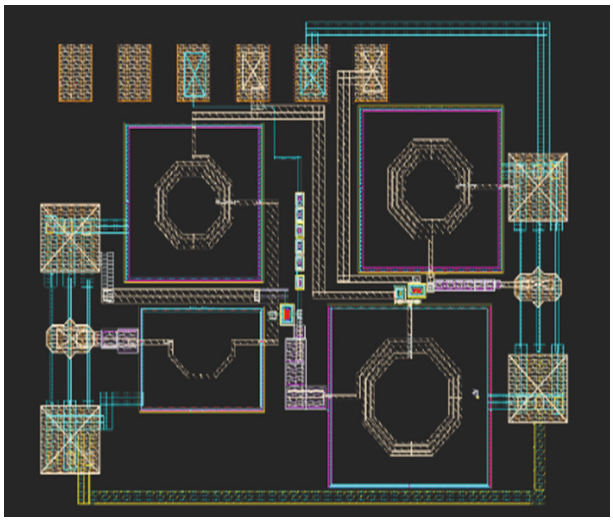


Fig. 10. Layout of the designed two-stage PA.

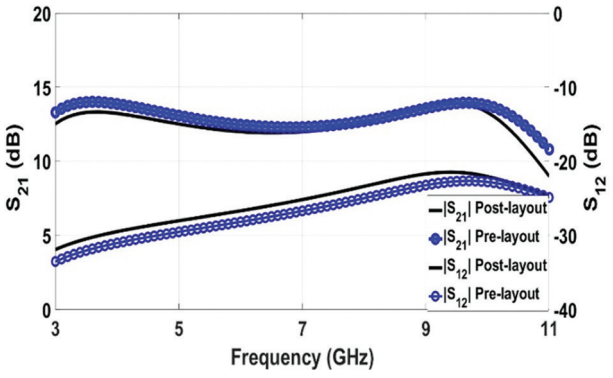


Fig. 11. Pre- and post-layout power gain ($|S_{21}|$) and reverse isolation ($|S_{12}|$) of the suggested UWB-PA.

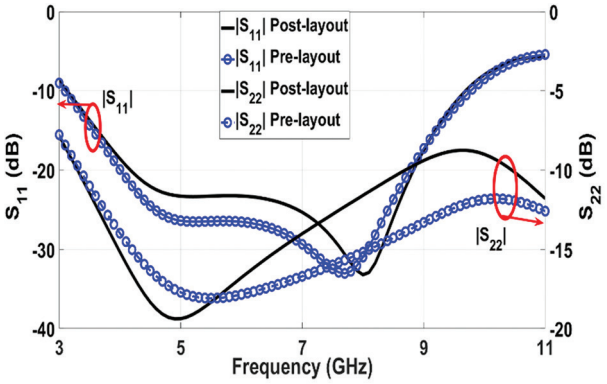


Fig. 12. Pre- and post-layout output return loss ($|S_{22}|$) and input return loss ($|S_{11}|$) of the suggested UWB-PA.

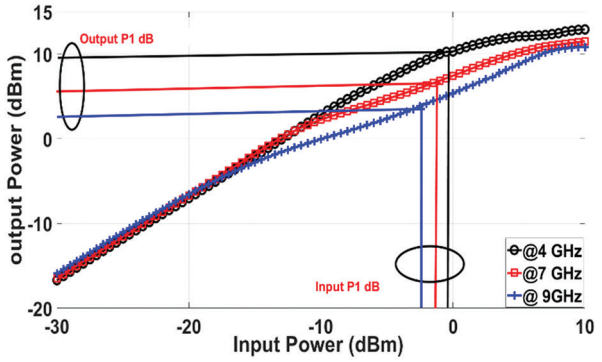


Fig. 14. Post-layout simulation result of the output power versus input power of the suggested UWB-PA.

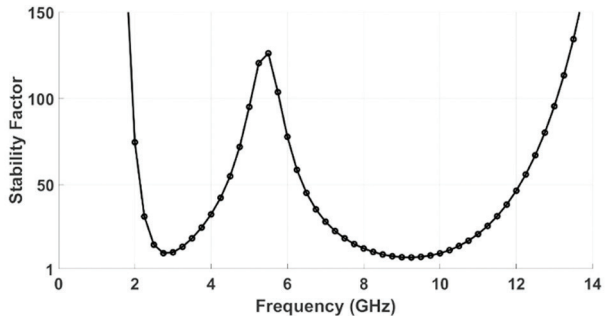


Fig. 16. Stability factor of the proposed PA.

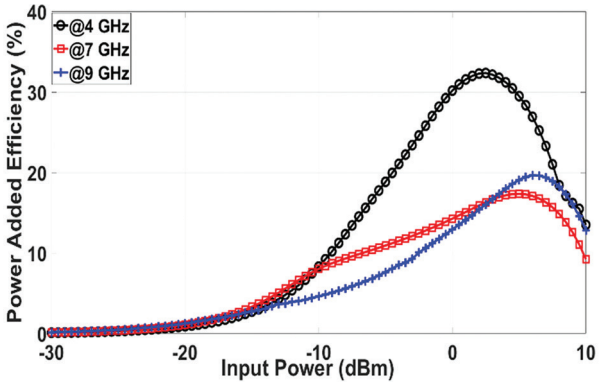


Fig. 13. Post-layout simulation result of PAE versus RF input power of the suggested UWB-PA.

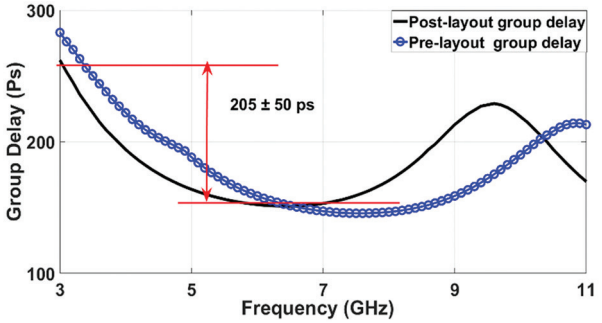


Fig. 15. Pre- and post-layout Simulation of GD variation of the suggested UWB-PA.

Table I summarizes the post-layout simulation results of the desinged PA and compares it's performance with the recently published UWB amplifers. Our proposed PA has good matching and gain flattness behaviour over the whole bandwidth, while providing high PAE and small group delay variation.

Moreover, the FOM[22, 29], given by Eq. 7, presents that the the proposed PA has a competitive performance compared to previous art.

$$FOM = \left(\frac{10^{Pout/10}}{1000}\right) * 10^{\frac{Gain}{10}} * F^2 * PAE \quad (7)$$

Table 1. Comparison of the designed PA post-layout simulation results with different published 0.18 µm CMOS UWB-PAs.

Ref.	CMOS Tech,	Freq. (GH)	S11 (dB)	S22 (dB)	Gain (dB)	GD (ps)	Max. PAE (%)	OP1dB (dBm)	Area (mm2)	DC Power	FOM
[6] 2021	45 nm	3.1-10.6	<-10	<-10	45± 0.5	NA	NA	10 @ 7 GHz	0.8	125	NA
[7] * 2019	130 nm	8-12	<-8	<-7	10	NA	29 @10 GHz	13@ 10 GHz	NA	20	578
[8] * 2015	180 nm	3.1-10.6	<-15	<-8	10	NA	10 @7 GHz	3 @ 7 GHz	0.9	15	10
[11] 2015	110 nm	8-12	<-5	<-7	9± 1.5	NA	20 @ 10 GHz	9 @ 10 GHz	0.66	NA	150
[12]* 2014	180 nm	3-5	<-7	<-8	13.3±1	NA	15 @ 4 GHz	1.5 @ 4 GHz	NA	25	12
[13] * 2013	180 nm	5-9	<-4	<-5	16±1	±20	13 @ 5 GHz	3 @ 5 GHz	0.6	25	33
[14] 2015	180 nm	5-10.6	<-5.5	<-7	14±1	±40	10 @ 8 GHz	3 @ 8 GHz	0.77	20	41

[15] * 2012	180 nm	5-11	<-9	<-9	11.5± 1	±41	18 @ 7 GHz	3.7 @ 7 GHz	0.96	18	44
[16] 2019	180 nm	3-10	<-8.5	<-10	11.5± 0.8	±68	26 @ 7 GHz	9 @ 7 GHz	0.8	34	156
[17] *2018	180 nm	3.1-10.6	<-6	<-7	15± 1	NA	22 @ 6 GHz	4 @ 6 GHz	0.53	15	80
[19] 2012	180 nm	3-10	<-9	<-13	11± 0.8	±85	NA	5 @ 6 GHz	0.77	100	NA
[21] 2017	65 nm	3-10	<-7	<-9	11± 2	±22	18 @ 6 GHz	15 @ 6 GHz	0.94	100	324
[22] 2018	180 nm	1.5-5	<-2	<-5	17±3	NA	22 @ 4 GHz	7 @ 4 GHz	1.2	25	140
[23] 2018	130 nm	6-9	<-8	<-9	9± 1	NA	22 @ 7 GHz	7 @ 7 GHz	0.86	24	56
[24] 2021	130 nm	7.8-11.5	<-9	<-5	8± 1	NA	20 @ 9 GHz	12 @ 9 GHz	1.1	58	162
This work*	180 nm	3.1- 10.6	<-4.5	<-8.5	12.5 ± 1.5	±50	32.5 @ 4 GHz	11 @ 9 GHz	0.55	36	165

*Simulated

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