Design and analysis of a new multi-level inverter topology with a reduced number of switches and controlled by PDPWM technique

Case Study

Fatima Chakir
IESI Laboratory, Department of Electrical Engineering, Faculty of Science and Technology, ENSET Mohammedia, Hassan II University Of Casablanca, Morocco, fatima.chakir5-etu@etu.univh2c.ma

Abdelmounime EL Magri
IESI Laboratory, Department of Electrical Engineering, Faculty of Science and Technology, ENSET Mohammedia, Hassan II University Of Casablanca, Morocco, magri_mounaim@yahoo.fr.

Rachid Lajouad
IESI Laboratory, Department of Electrical Engineering, Faculty of Science and Technology, ENSET Mohammedia, Hassan II University Of Casablanca, Morocco, rlajouad@gmail.com.

Mohamed Kissaoui
IESI Laboratory, Department of Electrical Engineering, Faculty of Science and Technology, ENSET Mohammedia, Hassan II University Of Casablanca, Morocco, kissaouimed@gmail.com

Mostafa Chakir
CED-ST, LESSI, Faculty of Sciences Dhar el Mehraz, Sidi Mohamed Ben Abdellah University, BP 1796, Fez-Atlas, 30003 Fez, Morocco, mostafa.chakir@usmba.ac.ma

Omar Bouattane
IESI Laboratory, Department of Electrical Engineering, Faculty of Science and Technology, ENSET Mohammedia, Hassan II University Of Casablanca, Morocco, o.bouattane@enset-media.ac.ma.

Abstract *– With their many advantages, including low power dissipation in power switches, low harmonic content, and reduced electromagnetic interference (EMI) from the inverter, multilevel converter (MLI) topologies are becoming more and more in demand in high and medium power applications. This paper introduces a novel multi-level symmetric inverter topology with adopted control. The objectives of this article are to architecturally define the positions of the various switches, to choose the right switches and to propose an inverter control strategy that will eliminate harmonics while producing the ideal output voltage/current. By using fewer switching elements, fewer voltage sources, and switches with a total harmonic content (THD) which reduces losses and a drop in minimum voltage (Vstrssj), the proposed topology is more efficient than conventional inverters with the same number of levels. The new topology will be demonstrated using a seven-level single-phase inverter. For various modulation indices, MATLAB-SIMULINK is used to study and validate the topology.*

Keywords*: Approximate controls, Inverter multi-level, Pulse with modulation (PWM),Total harmonic distortion (THD)*

1. INTRODUCTION

Renewable energy is an inexhaustible and freely available source of power. In addition to being viewed as ecologically clean and limitless on a human scale, sources like the sun's rays (solar energy), the wind (wind energy), and the kinetic energy of water (hydraulic energy) are used to produce so-called renewable energy.

Renewable energy is a cost-free and limitless energy source. Such resources as the solar, wind and kinetic energy of water are considered to be ecologically sound and, in theory, limitless on a human scale [1].

A good angle of inclination of the solar collector improves productivity and yield [2]. Since the energy produced by renewable sources is continuous and un-

stable [3], this causes instability in the production of electricity and contributes to the fidelity and quality of the electrical system. DC/AC converters are crucial to solve these problems [4].

The two most well-known types of classical structures are two-level inverters and three-level or modified square wave invertors. The latter, however, can be applied to specific applications [5], Due to their numerous drawbacks, such as their high harmonic rate, degraded fundamental voltage, large size, and extremely high rated switching voltage, they are not recommended for new projects [6, 7]. These problems were addressed by the design of multi-level inverters (MLI).

Multi-level inverters have received a lot of attention in recent years as a potential solution for high-power continues /alternative conversion applications. A PWM is a structure that connects various DC current or voltage sources (produced by a DC source, capacitors), power switches (MOSFET, IGBT), and results in the creation of a stepped waveform. At the terminals of the power switches, the voltage drops are smaller than the converter voltage as a whole[8] . Comparatively to conventional two-level inverters, multi-level inverters have a better harmonic profile of their output waveform [9, 10] . Moreover, fault-tolerant operation is possible [11]. The complexity and cost of the PWM configuration remain the main drawbacks due to the abundance of switching devices [12]. PWMs are frequently used for high and low power applications. The NPC(neutral-point clamped), the CHB (cascaded H-bridge), and the FC (flying capacitor inverter) are, however, the most well-known multilevel inverter topologies [13-17].

The new topology incorporates the same number of switches as the CHB topology which requires fewer switching elements compared to capacitor (CF) or diode (NPC) topologies, overriding the harmonic ratio of the voltage generated by the new topology (17.15%) is lower than that generated by the CHB (THBCHB = 18.3%) by adopting the same control technique (PDPWM) [18]. The new topology with its ability to generate an output voltage with a reduced harmonic content (compared to CHB) and a minimum number of switches (compared to FC and NPC) for the same number of levels, presents a good alternation by the reduction of switching losses since the number of the latter is reduced, its manufacturing cost and its size thus compared to the conventional converter, which attracts many researchers and industrial collaborators [7].

The article is structured as follows: Section II presented a generalized configuration of the proposed topology with mathematical formulations; this section also describes the operation mode of a single-phase, 7-level inverter. The modulation method (PWM) is introduced in section III. The results of the simulation are then presented in section IV. Section V compares the proposed topology and the traditional topologies in terms of the number of interrupters and THD. Conclusions are drawn in the final section.

2. THE SUGGESTIVE TOPOLOGY.

In this section, the structure of the new topology and its working principle for a single-phase seven-level PWM are presented. Formulas for voltage stresses across switches, output voltage, etc. are also presented.

2.1. THE NEW TOPOLOGY'S GENERAL STRUCTURE

The generalized structure of the new single-phase inverter topology is provided by (Fig. 1); it integrates n DC voltage sources connected in series by power switches.

The switches can be MOSFET or IGBT transistors with an antiparallel diode, connect the input sources Ej (where $j = 1$ to n) between them in order to produce the currents i_{1j} (t) and i_{2j} (t). IGBTs and antiparallel diodes are used in this inverter structure to model the power switches. In addition to two latch interrupts (S_1, S_2), complementary switches are identified by Q_{1j}, Q_{2j} (where $j = 1$ to n). v_{1j} $(t)/v_{2j}$ (t) (where j=1 to n) represents the voltage across the terminals of each switch. The symbols for load current and voltage are i_{ab} (t) and V_{ab} (t), respectively.

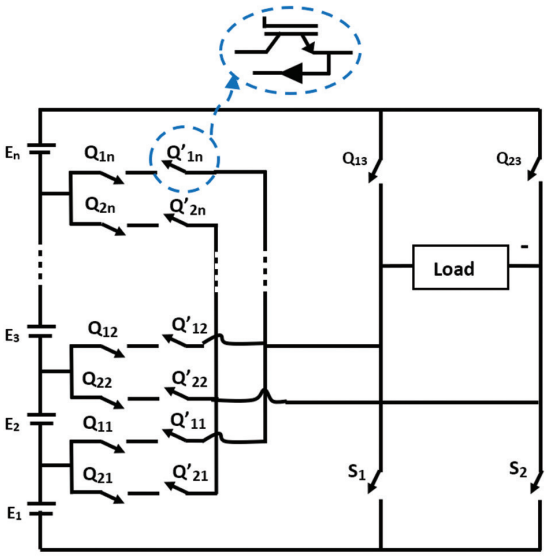


Fig. 1. The general proposed topology of the single-phase inverter

The new proposed symmetric topology of multi-level (SMLI) and mode of operation are shown in Fig. 2 and Table 1, respectively. For a 7-level output, it is necessary to use three voltage sources (E_1, E_2 and E_3) and twelve pairs of unidirectional switches, which are made up of IGBT transistors combined with an anti-parallel diode. The proposed topology results in a maximum voltage of $3E$ for the 7-level PWM:

$(E_1+E_2+E_3=3E)$.

Fig. 2 clearly shows that the combination of switches (Q_{13}, Q_{12}), (Q_{13}, Q_{11}), (Q_{13}, S_1), (Q_{12}, Q_{11}), (Q_{11}, S_1), (Q_{12}, S_1), (Q_{23}, Q_{22}), (Q_{23}, Q_{21}), (Q_{23}, S_2), (Q_{22}, Q_{21}), (Q_{21}, S_2) and (Q_{22}, S_2) in order to avoid short-circuiting of sources; those interrupter shouldn't be activated in the same time.

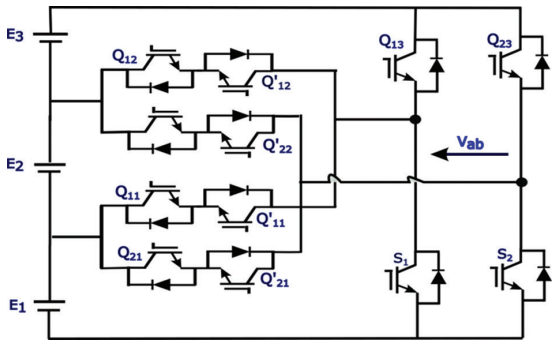


Fig. 2. The proposed topology for a 7-level symmetrical inverter

Table 1. The output voltage values Vab for different status of interrupters (F:OFF/ N:ON)

Level	State of switches								
	Q_{13}	Q_{12}	Q_{11}	S_1	S_2	Q_{23}	Q_{22}	Q_{21}	Vab
1	F	F	F	O	O	F	F	F	0
2	F	F	O	F	O	F	F	F	E
3	O	F	F	F	F	F	F	O	2E
4	O	F	F	F	O	F	F	F	3E
5	O	O	O	F	F	O	F	F	-E
6	F	F	F	O	F	F	O	F	-2E
7	F	F	F	O	F	O	F	F	-3E

A switch can present in more than one level structure to the output voltage in the single-phase inverter structure that is being proposed.

To achieve higher output voltage levels, the new inverter structure can be expanded.

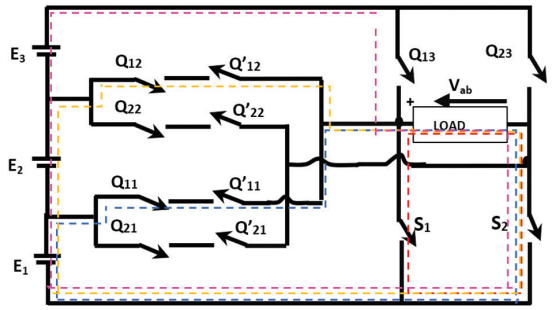


Fig. 3. Output voltage under operating mode of proposed topology: Vab=0; Vab=E; Vab=2E; Vab=3E;

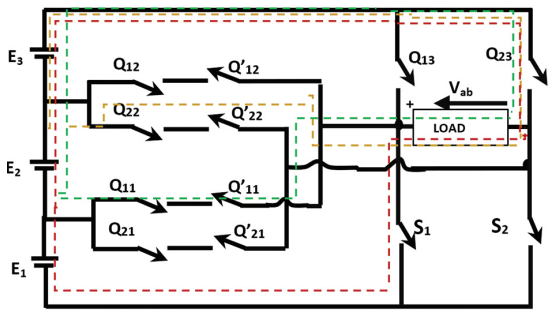


Fig. 4. Output voltage under operating mode of proposed topology: Vab= - E; Vab= -2E; Vab= -3E;

2.3. MATHEMATICAL FORMULATIONS

Based on the Fig.1, the switches Q_{1j} and Q_{2j} (j=1 to n) function in a complementary mode, the switching functions of Q_{1j}/Q_{2j} which are described as follows:

$$Q_{1j} = \begin{cases} 1, & if\ "ON" \\ 0, & if\ "OFF" \end{cases} \quad (1)$$

$$Q_{2j} = \begin{cases} 1, & if\ "ON" \\ 0, & if\ "OFF" \end{cases} \quad (2)$$

Then the load voltage v_{ab} (t) can be formulated using the nodal voltages v_a (t)and v_b (t) as:

$$\mathrm{V_{ab}(t) = V_a(t) + V_b(t)} \quad (3)$$

Or:

$$\mathrm{V_a(t) = Q_{1j} * j * E} \quad (4)$$

And:

$$\mathrm{V_b(t) = Q_{2j} * j * E} \quad (5)$$

By using (3), (4) and (5):

$$\mathrm{V_{ab}(t) = Q_{1j} * j * E - Q_{2j} * j * E} \quad (6)$$

Furthermore, the number of levels generated by the proposed typology is given by

$$\mathrm{N = 2 * n + 1} \quad (7)$$

Or:

n: is the number of continuous sources,

N: is the number of levels of the stepped output

The maximum voltage is given by:

$$\mathrm{V_{(max)} = n * E} \quad (8)$$

3. THE TECHNIQUES OF PWM MODULATION

The goal of modulation techniques is to create switch drive pulses that generate a voltage close to a sinusoidal shape at the output of the multilevel inverter (MLI) [18-19]. PWM techniques are used to reduce the harmonic level of the output wave and they can be classified as follows:

- APOD: Alternative Phase Opposition Disposition.
- PD: Phase Disposition Fig.5.
- POD: Phase Opposition Dispositions.

According to the literature, the PDPWM technique generates a better harmonic profile than the other methods (PDPWM & APODPWM) with a CHB inverter [18-21] , therefore, to validate the usefulness of the proposed topology, we will adopt the same technical (PDPWM) .

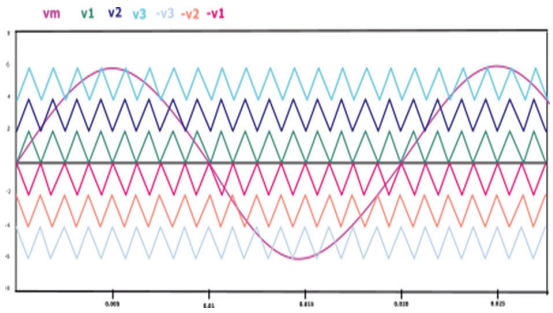


Fig. 5. The Phase Disposition techniques of PWM modulation

4. SIMULATION AND RESULTS

The MATLAB/Simulink tool was used; to examine the operation and inspected the results of the new topology. The latter is tested with the configurations already defined in Table 1 with the appropriate PDPWM command. The test parameters of the new 7-level DC/AC converter are given by Table 2. In this paper; two types of control are used: the full wave control to test the operation of the proposed topology -in the first time- and the PDPWM control in the second time. The aim is improving the performance of the output of our inverter (minimized the harmonic rate of the voltage and current produced).

Table 2. Simulation parameters

Input DC Voltage (V)	100
Charge Resistance R (Ω)	100
Charge Inductance L (H)	1e-1
Carrier signals (V)	100
carrier frequency (KHz)	4
Reference signal (V)	230
signal frequency (Hz)	50

a. Full Wave Control

The control of the switches are fixed according to the chronology given prior in the Table1. The output voltage wave and its total harmonic distortion realized using FFT analysis of MATLAB/Simulink are presenting in (Fig. 5).

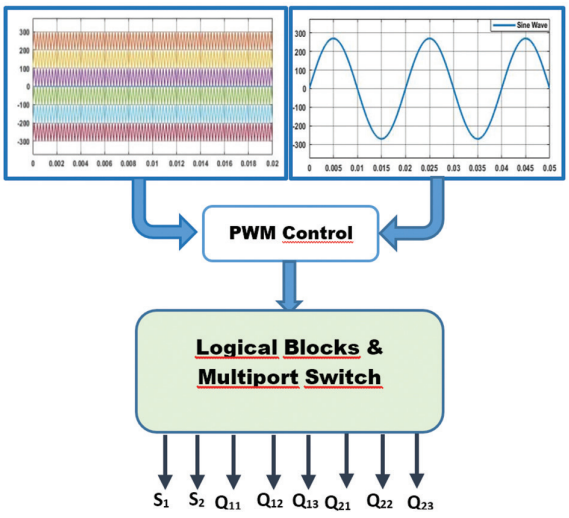
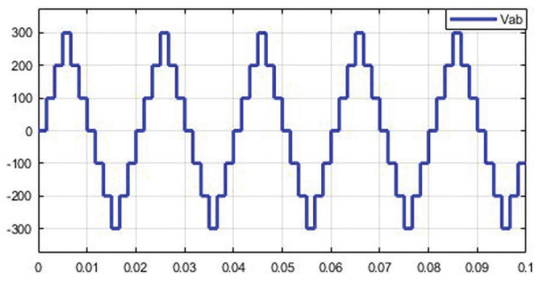
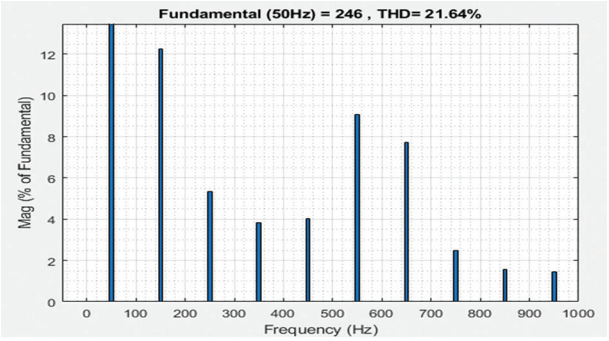


Fig. 6. Synoptic of the command adopted



(a)



(b)

Fig. 7. (a) Proposed seven- level output voltage waveform; **(b)** FFT analysis of voltage single phase MLI.

The THD of voltage output is 21.64 % with 3rd, 5th, 7th and 9th harmonics 12%, 5.6%, 3.8% and 4.03% respectively.

b. The multi-carrier PWM control.

References (sine waves) are compared to carriers (triangular waves). With F_{sin} and F_{tag} being the sine waveform and triangle waveform frequencies, respectively.

At first the values of V_{sin}, V_{tag} are: 230v, 100 v respectively; these last ones will be changed to obtain the different modulation index values. The carrier frequency used in the simulation is 10KHz.

V_{tag} is the amplitude of carrier signal;

V_{sin} is the amplitude of reference signal;

Then I_m is the modulation index is defined as:

$$\mathrm{I_m} = \frac{V_{sin}}{3 * V_{tag}} \tag{9}$$

The design goals of PWM inverters are to reduce the THD in the output current and voltage. To test the rate of harmonics, the simulations are carried out with an RL with (L=1$^{e\text{-}1}$) load and without using a filter. (Fig. 8) shows the current and voltage waveforms of our 7-level inverter as well as their THD for modulation indices from 0.6 to 1 with the same amplitude. Based on an analysis of the voltage and current waveforms exhibited by the new topology, the most appropriate output voltage profile (voltage and current close to the sinusoid) are given by a modulation index Im=0.8 (THDV=1.24% and THDI = 0.22% respectively). therefore, for the same number of output levels,we can see that the new topology generates a lower rate of harmonics than the topology proposed by [18], we constat that the new proposed topology generate a rate of current harmonics lower than the topology proposed by N.Motaparthi and all. in the two cases of study (without filter THDI=6.47% , with THDI= 2.89% filter) [22].

The Table 3 below; illustrates how the THD decreases with decreasing modulation index, resulting in fewer output voltage levels (I_m=0.6 generates 5 levels) Fig.8.a.

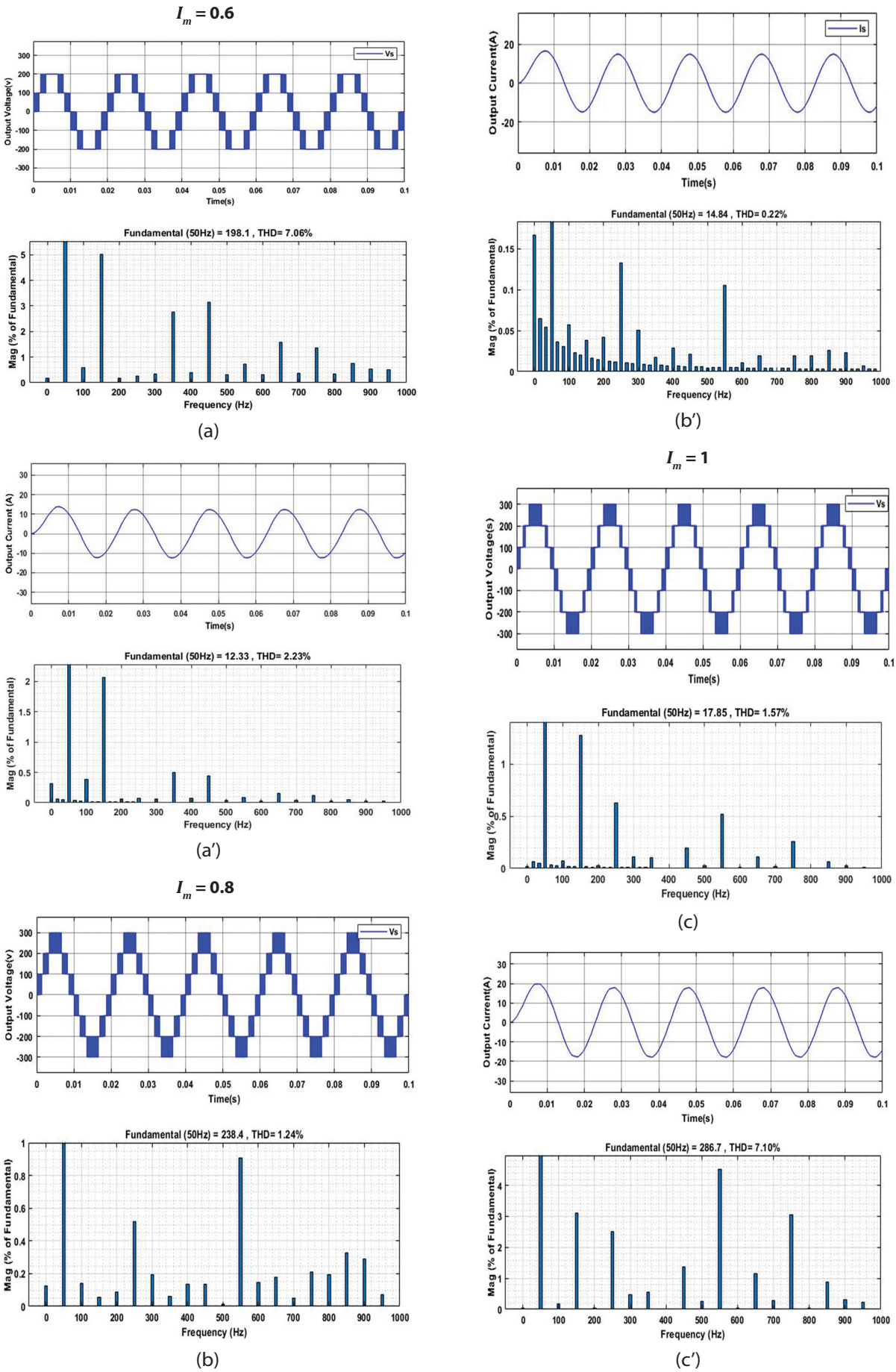


Fig. 8. Voltage, current waveforms generated by the new 7-level PWM and their THD at different modulation index: (a); (a')I_m=0.6, (b); (b')I_m=0.8, (c);(c')I_m=1

The design goals of PWM inverters are to reduce the THD in the output current and voltage. To test the rate of harmonics, the simulations are carried out with an RL_ with (L=1e^{-1}) load and without using a filter. (Fig. 8) shows the current and voltage waveforms of our 7-level inverter as well as their THD for modulation indices from 0.6 to 1 with the same amplitude. Based on an analysis of the voltage and current waveforms exhibited by the new topology, the most appropriate output voltage profile (voltage and current close to the sinusoid) are given by a modulation index I_m=0.8 (THDV=1.24% and THDI = 0.22% respectively). therefore, for the same number of output levels, we can see that the new topology generates a lower rate of harmonics than the topology proposed by [18], we constant that the new proposed topology generate a rate of current harmonics lower than the topology proposed by N.Motaparthi and all. in the two cases of study (without filter THDI=6.47% , with THDI= 2.89% filter) [22].

The Table 3 below; illustrates how the THD decreases with decreasing modulation index, resulting in fewer output voltage levels (I_m=0.6 generates 5 levels) Fig. 8. a.

Table 3. The variation of THD of voltage waveform as a function of different modulation index

Modulation Index	THDI% (THD of Current)	THDV% (THD of voltage)
0.6	2.23	7.06
0.7	0.44	2.23
0.8	0.22	1.24
0.9	0.69	3.81
1	1.57	7.1

5. COMPARATIVE STUDY

A comparison is presented in Table 4 between the new proposed topology , the Two-levels topology and three classics topologies: CHB, FC, and NPC [23-24].

Moreover, equation (7) gives the number of levels generated by the proposed topology.

The comparison between the new inverter topology, the two-level structure and the classic topologies: FC, CHB and NPC is given by Table 4, it is clear that the proposed symmetrical topology requires the same number of switches as the topology CHB presented in the article [23-24]; to generate particular output levels, on the other hand, it requires the minimum of components compared to FC and NPC topologies, as shown in table 4. we see that the new symmetrical structure does not need a flying capacitor and a clamping diode, which has an advantage of the latter over FC, NPC and the topologies presented in other literatures [6] because it reduces the complexity of the control circuit and avoids the balancing problem caused by the presence of the capacitors presented in the NPC and FC topologies. Looking at the THDs we notice that the topology has the lowest harmonic rate.

Therefore, the new proposed topology has proven to be the most efficient in producing voltage and current with the lowest THD while integrating the minimum number of switches compared to conventional topologies.

Table 4. Comparative study between the new proposed topology, two levels inverter and the classics structures according to the number of components

Components	Topologies				
	New Topology	NPC-MLI	FC-MLI	CHB-MLI	Two levels
DC Sources	(N-1)/2	1	1	(N-1)/2	1
Switches	2*(N-1)	2*(N-1)	2*(N-1)	2*(N-1)	2
Bus capacitors	0	(N-1)	(N-1)	0	1
Clamping diodes	0	2*(N+1)	0	0	0
Flying capacitors	0	0	(N+1)	0	0
Modulation technique	PD PWM	PD PWM	PD PWM	PD PWM	SVP PWM
THD(%) of current	0.22%	1.26%	4.22%	0.26%	6.02%
Total components for 7 levels inverter (N=7)	15	35	27	15	_

6. CONCLUSION

The purpose of this article is to present a new multilevel inverter topology that can be used in engineering applications. In this article, a single-phase 7-level inverter was used to validate and demonstrate the efficiency of the model. Researchers found that increasing output levels reduced total harmonic distortion (THD), but also increased losses and increased cost of the inverter as more switches were required. Therefore, our study focuses on developing a structure with a trade-off between the number of switches used and the number of output levels. Modulation index (I_m) variation influences inverter performance; for this reason the results of the simulation are presented for a different modulations indexes; varying from 0.6 to 1 for a good explanation of the results. Based on the FFT analysis of the output quantities (voltage/current) and comparing with previous studies, it appears that the topology produces a good voltage profile (THDV = 1.24%) for I_m = 0.8 without using additional filter. For the same number of output levels, the proposed topology appears to have the lowest THD for output voltage and current, therefore requires fewer components and therefore has less switching losses and does not include capacitors which exhibit the disadvantage of voltage balancing for classical topology. Consequently, the proposed topology is a good alternative for engineer applications.

Acknowledgements

This article is included in the UPISREE research project funded and supported by the organization Research in Solar Energy and New Energies (IRESEN).

7. REFERENCES:

[1] S. M. Shaahid, "Review of research on autonomous wind farms and solar parks and their feasibility for commercial loads in hot regions", Renewable and Sustainable Energy Reviews, Vol. 15, No. 8, 2011, pp. 3877-3887.

[2] X. Berisha, A. Zeqiri, D. Meha, "Determining the Optimum Tilt Angles to Maximize the Incident Solar Radiation - Case of Study Pristina", International Journal of Renewable Energy Development, Vol. 7, No. 2, 2018, pp. 123-130.

[3] B. P. Chandran, A. I. Selvakumar, F. M. Mathew, "Integrating multilevel converters application on renewable energy sources—A survey", Journal of Renewable and Sustainable Energy, Vol. 10, No. 6, 2018, p. 065502.

[4] K. Dhineshkumar, C. Subramani, A. Geetha, C. Vimala, "Performance analysis of PV powered multilevel inverter", International Journal of Electrical and Computer Engineering, Vol. 9, No. 2, 2019, p. 753.

[5] W. Phetphimoon, Y. Kongjeen, K. Bhumkittipich, "Design of High-Frequency ZVS Full-Bridge Power Converter for Photovoltaic Applications", International Review of Electrical Engineering, Vol. 16, No. 6, 2021, p. 497.

[6] K. K. Gupta, S. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources", IEEE Transactions on Industrial Electronics, Vol. 61, No. 7, 2014, pp. 3269-3278.

[7] A. Dekka, A. Ramezani, S. Ounie, M. Narimani, "A New 5-Level Voltage Source Inverter", Proceedings of the IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, March 2019, pp. 2511-2515.

[8] S. F. Mekhamer, R. H. Shehata, A. Y. Abdelaziz, M. A. Al-Gabalawy, "Enhancing radial distribution system performance by optimal placement of DSTATCOM", International Journal of Electrical and Computer Engineering, Vol. 10, No. 3, 2020, p. 2850.

[9] S. Choudhury, M. Bajaj, T. Dash, S. Kamel, F. Jurado, "Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects", Energies, Vol. 14, No. 18, 2021, p. 5773.

[10] S. Raj, R. K. Mandal, M. De, A. K. Singh, "Nine-level inverter with lesser number of power semiconductor switches using dSPACE", International Journal of Power Electronics and Drive Systems, Vol. 13, No. 1, Mar. 2022, p. 39.

[11] G. Buticchi, E. Lorenzani, G. Franceschini, "A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems", IEEE Transactions on Industrial Electronics, Vol. 60, No. 3, 2013, pp. 906-918.

[12] A. M. Al-Mahrouk, N. F. Mailah, M. A. Mohd Radzi, M. K. Hassan, "Systematic Review of Multilevel and Matrix Usage in Power Electronics: Circuit Types, System Taxonomy, Applications and Recommendations", International Review of Electrical Engineering, Vol. 15, No. 2, 2020, p. 108.

[13] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review", IEEE Transactions on Power Electronics, Vol. 30, No. 1, 2015, pp. 37-53.

[14] D. Roy, M. Singh, "A Single Z-Source Network-Based 3-Level NPC Inverter Using a Novel Region Selection Approach of SVM", International Review of Electrical Engineering, Vol. 15, No. 5, 2020, p. 394.

[15] M. Malinowski, K. Gopakumar, J. Rodriguez, M. A. Pérez, "A Survey on Cascaded Multilevel Inverters", IEEE Transactions on Industrial Electronics, Vol. 57, No. 7, 2010, pp. 2197-2206.

[16] K. Compala Lakshmiah, T. A. Raghavendiran, "A New Modified H-Bridge Multilevel Inverter with Multi Carrier PWM Technique for Speed Control of Induction Motor", International Review of Electrical Engineering, Vol. 13, No. 5, 2018, p. 365.

[17] F. Gülpınar, F. Sarı, Y. Uzun, "Analysis of a Novel Four Level Flying Capacitor H - Bridge Converter", International Journal of Renewable Energy Development, Vol. 7, No. 1, 2018, p. 71.

[18] C. Manivelan, "A Survey on Multilevel Inverter Topologies and Control Schemes with Harmonic Elimination", Proceedings of the International Conference on Electrotechnical Complexes and Systems, Ufa, Russia, October 2020, pp. 1-7.

[19] W.-K. Choi, F. Kang, "H-bridge based multilevel inverter using PWM switching function", Proceedings of the 31st International Telecommunications Energy Conference, Incheon, South Korea, October 2009, pp. 1-5.

[20] S. W. Shneen, F. N. Abdullah, D. H. Shaker, "Simulation model of single phase PWM inverter by using MATLAB/Simulink", International Journal of Power Electronics and Drive Systems, Vol. 12, No. 1, 2021, p. 212.

[21] R. Taleb, M. Helaimi, D. Benyoucef, Z. Boudjema, "A comparative analysis of multicarrier SPWM strategies for five-level flying capacitor inverter", Proceedings of the 8th International Conference on Modelling, Identification and Control, Algiers, Algeria, November 2016, pp. 608-611.

[22] N. Motaparthi, K. Kumar Malligunta, "Seven-Level Symmetrical Series/Parallel Multilevel Inverter with PWM Technique Using Digital Logic", International Journal of Electrical and Computer Engineering Systems, Vol. 12, No. 3, 2021, pp. 123-130.

[23] R. Mali, N. Adam, A. Satpaise, A. P. Vaidya, "Performance Comparison of Two Level Inverter with Classical Multilevel Inverter Topologies", Proceedings of the IEEE International Conference on Electrical, Computer and Communication Technologies, Coimbatore, India, February 2019.

[24] S. P. Gautam, "Novel H-Bridge-Based Topology of Multilevel Inverter With Reduced Number of Devices", IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 7, No. 4, 2019, pp. 2323-2332.