Performance Investigation of 17 Level Reduced Switch Count Multilevel Inverter

Original Scientific Paper

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Abstract *– The primary objective of this paper is to introduce a 17-level multilevel inverter with only eight power switches and three diodes that can be suitable for electric vehicle applications. This setup utilizes three distinct unequal DC sources to create the 17 levels of output voltage waveforms. The modes of operations of the proposed topology have been discussed in detail. The calculation of conduction losses, switching losses, efficiency, total standing voltage, and cost function per level for the suggested inverter has been elaborated. Due to more semiconductor power switches, diodes, capacitors, driver circuits, and DC sources in typical inverters, switching losses, costs, and harmonic distortion are increased. The nearest-level control technique has been utilized to control the switching elements of the recommended configuration. The performance comparison of various multilevel inverter topologies has also been discussed. The suggested multilevel inverter provides a higher efficiency of 98.60%, cost function of 3.6 for a weight coefficient of 1, improved power quality, and higher reliability. A reduction in the power switches significantly reduces the convolution of switching circuitry. The total harmonic distortion produced by this inverter is 3.49%, which comes under the IEEE standard of 5%.*

Keywords: *Multilevel Inverter, Electric Vehicle, Nearest Level Control, Total Harmonic Distortion, Pulse Width Modulation*

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1. INTRODUCTION

Multilevel inverters are generally used in smart grids, battery-powered electric vehicles (EVs), and FACTS devices because of attributes including higher power quality, enhanced adaptability, and lessened dv/dt stress. Due to their capacity to generate high terminal output voltages employing low and medium voltage components, they are highly suited for the aforementioned purposes [1, 2]. Multilevel inverters (MLIs) are generally classified as one of the three types: diode clamped or neutral point clamped multilevel inverters (NPCMLI or DCMLI), flying capacitor multilevel inverters (FCMLI), and cascaded H-bridge multilevel inverters (CHBMLI). Diodes are mainly used in this inverter for clamping voltage, so it is called DCMLI, which demands more diodes and power components when the output waveform levels rise, which complicates circuit control. By using the redundancy in switching states offered by clamping capacitors, the voltage balancing problem caused by diodes in DCMLI can be resolved in FCMLI. Capacitors are used as clamping components, so it is called FCMLI; however, higher passive circuit components would decrease circuit reliability [3-6]. Compared to the other two MLIs, a MLI that consists of serially connected or cascaded H-bridges, called CHBMLI, is enormously modular and easier to control. Furthermore, it eliminates the necessity for voltage balancing circuits by using devoid DC sources. However, in the typical CHBMLI, each additional DC source enhances the need for four power electronic switches [7]. A unique multilevel inverter arrangement has been pre-

sented with n+5 power switches and 'n' independent sources for high levels. The standing voltage across the power switches in the polarity changer increases significantly as a result of the elevated levels in the terminal voltage waveform. Power switches with the highest voltage and the largest heat sinks must be used [8, 9]. The overwhelming majority of structures that rely on autonomous DC sources for producing levels in output waveforms are based on the idea of using switched DC input voltages to add level and polarity flipping using H-Bridge. The number of elements rises since the total blocking output across the H-Bride is four times the DC input voltage [10-12]. A framework that incorporates a four-quadrant power switch design, enabling both balanced and unbalanced switching circuit operation. The configuration features a large number of power switches, which increase losses [13]. MLIs have gained popularity in a variety of low- to high-voltage, high-power applications because of their unique features. Improved power quality, less electromagnetic interference, decreased voltage stress, and semiconductor device loss are a few merits of MLIs. Three key issues with MLIs are high precision control, an increase in power semiconductor switches and capacitors, and voltage balancing [14-17]. MLIs have not yet been extensively employed in low-power electric transportation, even though they have been used in traction drives in a number of experiments. These arrangements are seen in low-power automobiles like electric buses and passenger EVs, as well as high-power electric trains and ships. They use a standard two-level inverter because of its low DC-link voltage, simplicity in design, and convenience of use [18-22]. Eleven switches, three capacitors, three diodes, and one source of seven-level SCMLI are implemented. The capacitors in this configuration are self-balanced. However, the overall circuitry complexity is higher due to more switches, diodes, and capacitors [23]. Six switches, two diodes, and two sources of 5 level MLI have been introduced for renewable energy applications [24]. Seven switches, three diodes, and three sources of 15 level MLI have been discussed [25]. Ten switches, three diodes, and three capacitors with 13 level MLI have been introduced [26]. Eight switches, two sources 11 level inverter have been employed [27].

This work provides a new reduced switch count multilevel inverter (NRSCMLI) that combines a multi-conversion cell and H-bridge. The proposed MLI is very compact and requires only 8 switches, 3 diodes, and 3 unequal DC voltage sources. The nearest level control (NLC) technique is designed for this inverter. A comparative study has been done based on the number of switches, diodes, driver circuits, capacitors, and DC sources, total blocking voltage per unit, and cost function per level for 17 levels of various existing MLIs. The suggested configuration's key design feature has fewer components for seventeen levels when compared to conventional MLIs.

2. CONVENTIONAL MULTILEVEL INVERTERS

NPCMLI, or DCMLI, has been used to create a multilevel output voltage, which is shown in Fig. 1a. To achieve the needed output levels, power switches are placed in series, with diodes functioning as clamping elements. NPCMLI has minimised expenses and is more adjustable since it uses diodes for clamping. To accomplish a waveform with'm' levels in the output voltage or current, (m-1) DC-link capacitors are required. Each phase desires 2(m−1) power semi-conductor switches and (m−1) (m−2) diodes. There is an unbalanced stress on switches throughout the operation of NPCMLI. It requires more diodes and power switches. Moreover, this NPCMLI elevates the inverter power while needing one central and one high DC-link voltage [2, 3]. The next design, FCMLI, is seen in Figu. 1b. It employs flying capacitors in place of clamped diodes and delivers a clean output waveform while being safer and easier to operate. Because capacitors are used as clamping elements in the FCMLI, it is also simple to regulate. Every switch in this MLI shares the same amount of power dissipation.

Higher switching frequencies and balanced clamping capacitor voltages at high DC-link voltages are essential for the FCMLI. Since capacitors are more costly than diodes, this inverter is more complex and expensive than NPCMLI [4]. Alternatively, CHBMLI topology is one type of MLI that involves multiple symmetrical DC sources with H-bridges, as shown in Fig. 1c. The same circuit with unequal sources is specified as a hybrid MLI, as shown in Fig. 1d. Each H-bridge comprises four power switches [15]. Fig. 1e and Fig. 1f display the new cascaded MLI, which encompasses two stages; the first stage is two switches with equal or unequal DC sources, which can be prolonged effortlessly to create more levels. The second stage is the H-bridge, which converts the stepped direct current waveform into an alternate current waveform. Figure 1g shows a circuit diagram of a modified reduced switch count MLI, which consists of a multi-conversion cell and an H-bridge. A multi-conversion cell has only 4 switches and 4 power diodes with 4 equal DC sources. A multi-conversion cell is serially connected to an H-bridge for AC conversion. Figure 1h shows the circuit diagram of a modified hybrid multilevel inverter with unequal DC sources [25].

3. NEW REDUCED SWITCH COUNT MULTILEVEL INVERTER

The layout of the recommended structure, comprising four power switches and three unequal voltage sources ($1V_{DC}$, $2V_{DC}$, and $5V_{DC}$) is illustrated in Fig. 2. The unequal voltage sources are created by 1:1, 1:2, 1:5 transformers and DC-DC converters. This proposed structure produces a unidirectional stepped 17 level output voltage or current waveform. It is further connected to the H bridge circuit to create an alternate output waveform. Fig. 3 displays the overall construction of the proposed NRSCMLI. The significant benefit of the recommended MLI is that it has 17 levels while using only 8 power switches. The operation of the proposed multilevel is;

Mode 1: Devices S_5, S_6, S_7 & S_8 conduct, and it creates zero output voltage.

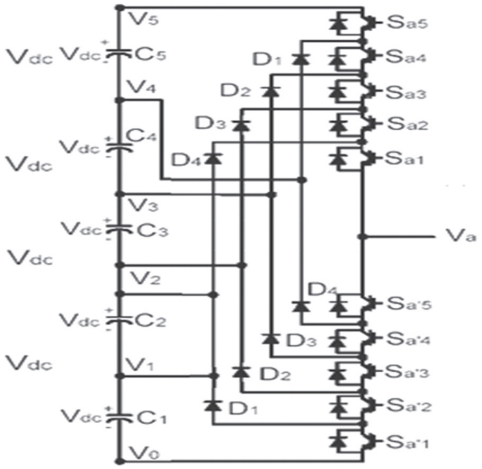
Mode 2: Switches S_1, S_5, S_8, D_2 & D_3 conduct and generate $1V_{dc}$=28V, it supplies to the load.

Mode 3: Switching elements S_2, S_5, S_8, D_1 and D_3 conduct and producing $2V_{dc}$=56V, it supplies the load.

Mode 4: Power switches S1, S2, S5, S8, D3 & D4 conduct and generate $1V_{dc}+2V_{dc}=3V_{dc}$.

Mode 5: In this operating mode, switches S4 and D1 conduct and produce $5V_{dc}-1V_{dc}=4V_{dc}$=112V to load.

Mode 6: Device S_3 only conducts along with diodes D_1 and D_2 and produces $1V_{dc}+5V_{dc}=5V_{dc}$=140V.



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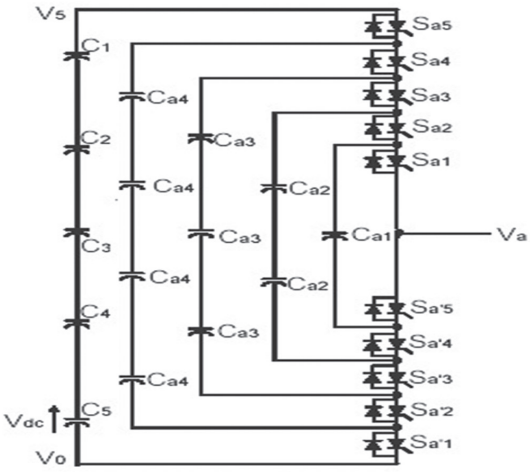

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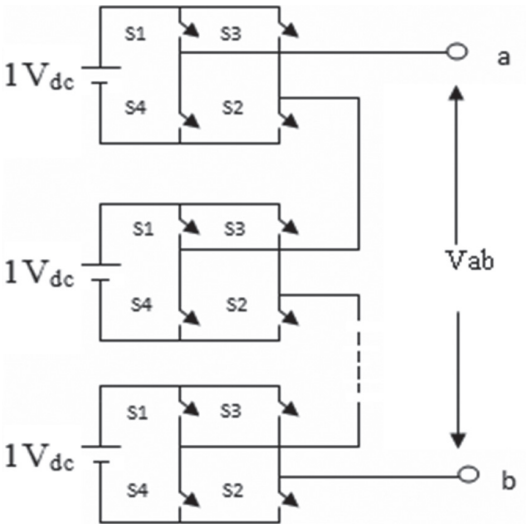

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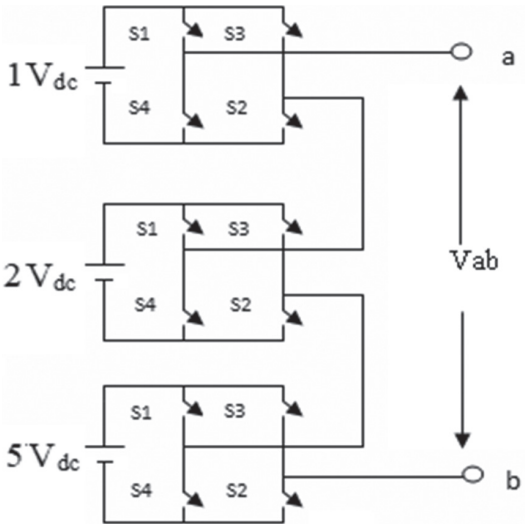

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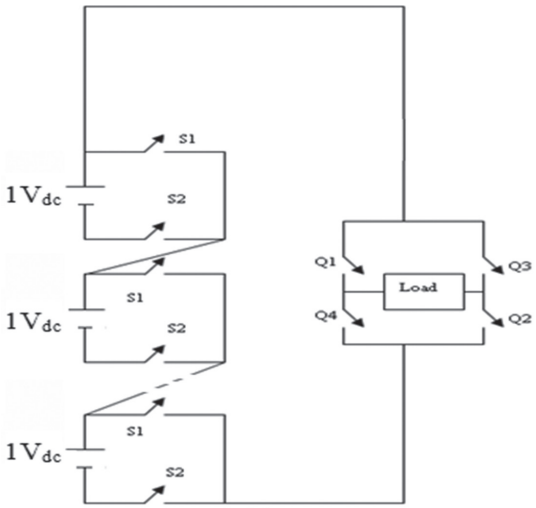

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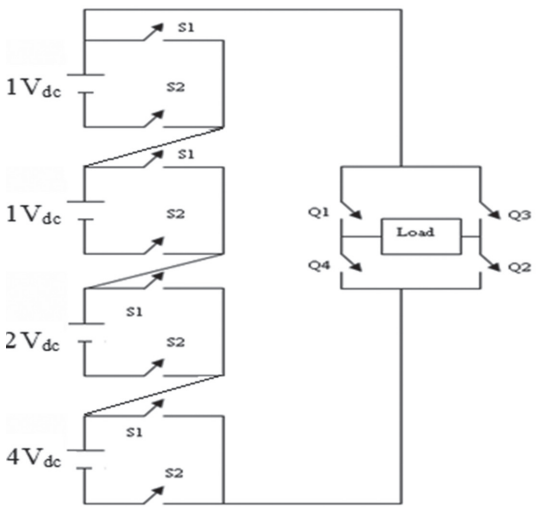

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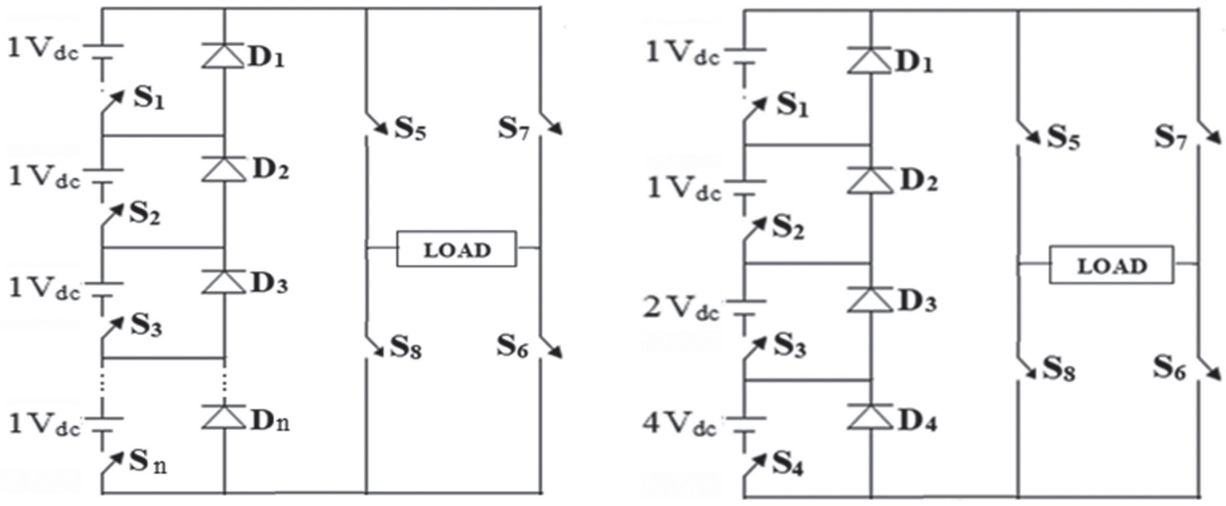

Fig. 1. a) Diode Clamped MLI, b) Flying Capacitor MLI, c) Cascaded H bridge MLI, d) Hybrid MLI, e) New Cascaded MLI, f) New Hybrid MLI, g) Modified Cascaded MLI, h) Modified Hybrid MLI. [2-4, 15, 25]

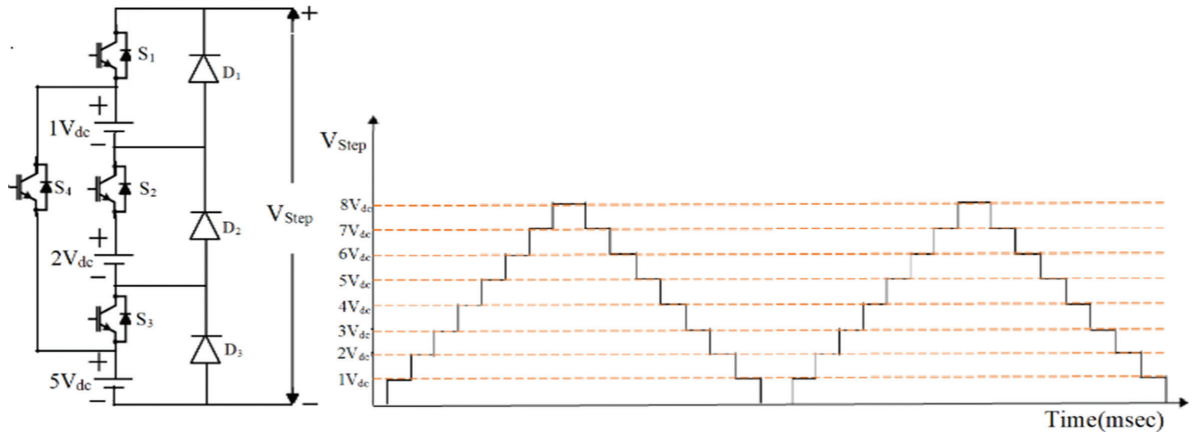

Fig. 2. Multi-Conversion Cell for New Reduced Switched Count multilevel inverter

Mode 7: Switches $S_{1'}$ $_{S3}$, and D_2 conduct and generates $1V_{dc}+5V_{dc}=6V_{dc}=168V$.

Mode 8: Elements S_2, S_3, and D_1 conduct and give $2V_{dc}+5V_{dc}=7V_{dc}=196V$ to the load.

Mode 9: Switches S_1, S_2, S_3 conduct, and the voltage across the terminal is $1V_{dc}+2V_{dc}+5V_{dc}=8V_{dc}=224V$.

Mode 10: Switches S_2, S_3, and D_1 conduct and create $2V_{dc}+5V_{dc}=7V_{dc}=196V$, supplies to the load.

Mode 11: Switches S_1, S_3 and D_2 conduct, and the load output voltage is $1V_{dc}+5V_{dc}=6V_{dc}=168V$.

Mode 12: Switches S_3, D_1 and D_2 conduct, and voltage across the load is $5V_{dc}=140V$.

Mode 13: Switches S_4 and D_1 conduct, and the output voltage is $5V_{dc}$-$1V_{dc}=4V_{dc}=112V$.

Mode 14: Power switches S_1, S_2, S_5, & S_8 and D_3 conduct, and the developed load voltage is $1V_{dc}+2V_{dc}=3V_{dc}=84V$.

Mode 15: Devices S_2, S_5, S_8, D_1 and D_3 conduct, and the developed output voltage is $2V_{dc}=56V$.

Mode 16: Switches S_1, S_5, S_8, D_2 and D_3 conduct, and the circuit generates $1V_{dc}=28V$ for the load.

Mode 17: In this mode, S_5, S_6, S_7 & S_8 conduct, and it produces zero voltage. Mode 1 to 17 give a 17 level output voltage for a positive half cycle. The same modes are repeated to generate a negative half cycle also but switches S_6 and S_7 conduct instead of switches S_5 and S_8. Fig. 6 and Table 1 display the modes of operation of the suggested MLI.

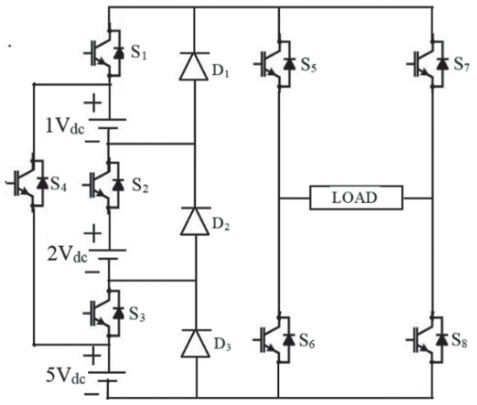

Fig. 3. Proposed New Reduced Switched Count multilevel inverter

4. ESTIMATION OF LOSS AND EFFICIENCY

This part describes the theoretical calculation of losses used to determine the efficiency of the recommended inverter. Conduction and switching losses are the most significant losses, and their computation relies on the assumption that the load is completely resistive and that the voltage at the inverter's output terminal resembles a staircase output waveform. When MOSFET power switches in a MLI are activated and conduct electricity, conduction loss occurs. The overall loss during conduction in the suggested inverter architecture is calculated for each MOSFET power switch. The same has been calculated for the polarity transformation unit separately. Power switches are employed as a polarity conversion unit in the proposed inverter, and load current in a single phase is observed with respect to neutral. In this case, the loss due to the switch conduction period during the basic cycle quarter is calculated.

$$P_{CON} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} {I_R}^2(t)\, R_{ON,}Tdt \tag{1}$$

The transistor's on-state resistance and load current are symbolized as $R_{on}T$ and $I_R(t)$ respectively. By engaging a high number of auxiliary units, the projected system delivers 17 levels of output voltage and current in the load side. As a result, the load current is stated as

$$I_R = I_{P,}sinwt \tag{2}$$

The average loss of a single-phase system during conduction is estimated using (1) and (2) as,

$$P_{CON1} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} {I_{P,}}^2 sin^2\, wtR_{ON,}Tdt \tag{3}$$

The multi-conversion unit's MOSFET switches are active during the basic cycle. The losses of multi-conversion for the 'π' cycle period is as

$$P_{CON2} = \frac{1}{\pi}\int_0^{\pi} {I_{P,}}^2 sin^2\, wtR_{ON,}Tdt \tag{4}$$

The loss during conduction is computed using the following equation for the single multi-conversion unit in the proposed MLI.

$$P_{CON,TOTAL} = P_{CON1} + P_{CON2} \tag{5}$$

In MOSFET power switches, switching loss occurs by the overlap of voltage and current during the ON/OFF or vice versa transition. The following formula is used to estimate the energy loss of MOSFET power switches during their on and off times.

$$E_{ON} = \frac{V_{ON}\times I}{6}\, T_{ON} \tag{6}$$

where V_{ON} - on-state voltage, I - current after switching on, T_{ON} - turn on time.

$$E_{OFF} = \frac{V_{OFF}\times I}{6}\, T_{OFF} \tag{7}$$

V_{OFF} - off-state voltage of MOSFET, I_{OFF} - current passing through the MOSFET before it turns on, and T_{OFF} - turn-off time. Using equations (6) and (7), the switching loss in the predicted MLI is calculated separately for each power switch in each unit. After half of the fundamental cycle, the MOSFET power switches in the polarity conversion unit are turned on and off, and the switching loss is calculated as follows.

$$P_{SW1} = 2\times f\times (E_{ON} + E_{OFF}) = \frac{1}{3}\times f\times I\times (V_{ON}T_{ON} + V_{OFF}T_{OFF}) \tag{8}$$

The fundamental switching frequency is f. Likewise, the switching loss of a multi-conversion unit is considered as throughout the half time. It is specified by,

$$P_{SW2} = 2\times f\times (E_{ON} + E_{OFF})f\times I(V_{ON}T_{ON}V_{OFF}T_{OFF}) \tag{9}$$

For a full cycle, the overall switching loss can be inferred as

$$\mathrm{P_{SW,TOTAL}} = \mathrm{f}\times(\mathrm{P_{SW1}} + \mathrm{P_{SW2}}) \tag{10}$$

The power loss of the NRSCMLI is computed by using (11)

$$P_{LOSS,,TOTAL} = P_{CON,T} + P_{SW,T} \tag{11}$$

The efficiency is calculated by using the following formulae

$$Efficiency = \frac{P_{OUT}}{P_{out}+P_{LOSS,T}}\times 100\% \tag{12}$$

The calculations show that the efficiency of the 17-level NRSCMLI is 98.60%, its conduction losses are 10.24W, its switching losses are 0.36W, its input power is 756.7W, its output power is 746.1W.

5. NEAREST LEVEL CONTROL(NLC) FOR 17 LEVEL NEW REDUCED SWITCH COUNT MULTILEVEL INVERTER

NLC is a common approach used in modular multilevel converters. Low switching frequency control technology known as NLC or the round approach is adaptable and simple to use. The semiconductor switches of the converter are activated by the appropriate gating signals produced by the NLC approach. Take the basic sinusoidal function with unit magnitude multiplied by the modulation index as a starting point. Allow the resulting signal to pass through the inverter's total positive levels (N) after that. Employ the round function next to obtain the necessary levels. The round function serves effectively to decrease switching losses by causing just one commutation to occur between two voltage steps, as shown in Fig. 4. Considering a Vref, the modulation index 'm' the nearest voltage level that can be estimated as follows:

$$V_{ref}=\mu\left(\frac{L-1}{2}\right)Vsin(wt) = V_m\sin(wt)$$
$$m = \frac{V_m}{\left(\frac{L-1}{2}\right)V},\ V_m = Vround\left(\frac{V_{ref}}{V}\right) \tag{13}$$

V_{ref} - reference sinusoidal voltage
L - number of levels
m - modulation index
V_m – peak ac voltage
V_{dc} – voltage difference between two levels

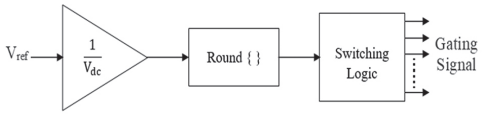

Fig. 4. NLC control method

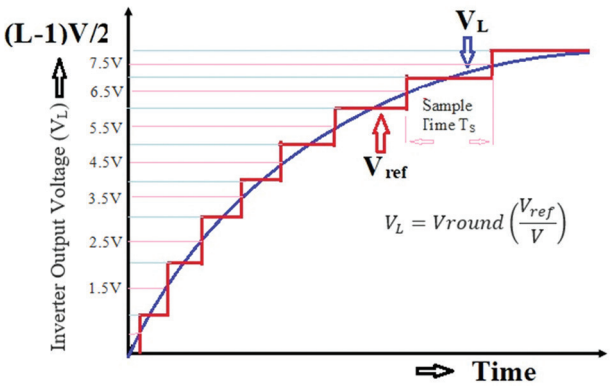

Fig. 5. NLC technique synthesis for 17 level

Fig. 5 indicates the identification of the nearest voltage level and the principle of the NLC method for the projected 17 level inverter.

6. RESULTS AND DISCUSSIONS

Fig. 7 shows the simulation diagram of NRSCMLI, Fig. 8 depicts the switching pulses of NRSCMLI; and Fig. 9 shows the MATLAB simulated output voltage waveform of the 17-level proposed MLI for a resistive load of 10 kW. The magnitude of the voltage is 224V, and the current is 44 A. Fig. 10 shows the output voltage and current waveform for a resistive (R) and inductive (L) load of 11 KVAR. The magnitude of the current is 50 A and the nature of the current waveform is sinusoidal. Fig. 11 shows the output voltage and current waveform for parallel resistive and inductive loads. From this figure, it clearly indicates that the nature of the output current waveform is sinusoidal for R and RL loads. From the Fast Fourier Transform (FFT) analysis window, it is understood that while the levels are raised, harmonics and THD are minimized. Fig. 12 shows that for the 17-level inverter, the voltage THD value is 3.49%. A simulation result of NRSCMLI is validated by the hardware prototype. Four MOSFETs (IRF250) are connected to form a multi conversion cell, and it is connected to an H-bridge, which comprises four MOSFETs. 3 unequal DC sources are attained by using specially designed 3 separate transformers in the ratios of 1:1, 1:2 and 1:5. Input for the all transformer is 28V. The AC output of transformers is converted into DC voltages by using rectifiers. A PIC 16F877 microcontroller is employed as the primary processor, it delivers gate trigger signals.

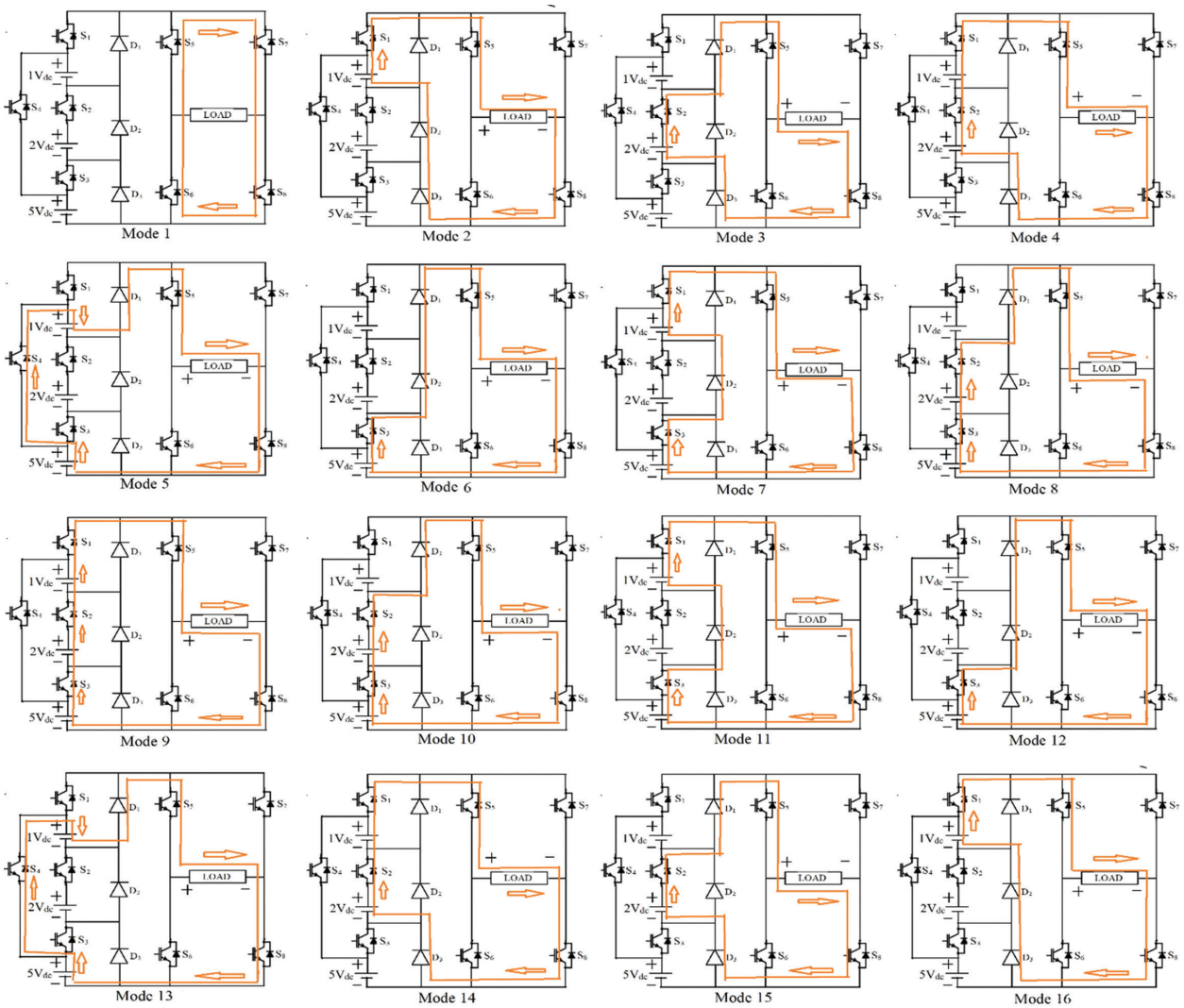

Fig. 6. Operation of New Reduced Switched Count multilevel inverter

Table 1. Operation of Proposed Multilevel Inverter

	Modes	Load Current Path											Output Voltage(V)	
		S1	S2	S3	S4	S5	S6	S7	S8	D1	D2	D3		
Positive Half Cycle	1	0	0	0	0	1	1	1	1	OFF	OFF	OFF	0Vdc	0V
	2	1	0	0	0	1	0	0	1	OFF	ON	ON	1Vdc	+28V
	3	0	1	0	0	1	0	0	1	ON	OFF	ON	2Vdc	+56V
	4	1	1	0	0	1	0	0	1	OFF	OFF	ON	3Vdc	+84V
	5	0	0	0	1	1	0	0	1	ON	OFF	OFF	4Vdc	+112V
	6	0	0	1	0	1	0	0	1	ON	ON	OFF	5Vdc	+140V
	7	1	0	1	0	1	0	0	1	OFF	ON	OFF	6Vdc	+168V
	8	0	1	1	0	1	0	0	1	ON	OFF	OFF	7Vdc	+196V
	9	1	1	1	0	1	0	0	1	OFF	OFF	OFF	8Vdc	+224V
	10	0	1	1	0	1	0	0	1	ON	OFF	OFF	7Vdc	+196V
	11	1	0	1	0	1	0	0	1	OFF	ON	OFF	6Vdc	+168V
	12	0	0	1	0	1	0	0	1	ON	ON	OFF	5Vdc	+140V
	13	0	0	0	1	1	0	0	1	ON	OFF	OFF	4Vdc	+112V
	14	1	1	0	0	1	0	0	1	OFF	OFF	ON	3Vdc	+84V
	15	0	1	0	0	1	0	0	1	ON	OFF	ON	2Vdc	+56V
	17	1	0	0	0	1	0	0	1	OFF	ON	ON	1Vdc	+28V
	18	0	0	0	0	1	1	1	1	OFF	OFF	OFF	0Vdc	0V
Negative Half Cycle	19	0	0	0	0	1	1	1	1	OFF	OFF	OFF	0Vdc	0V
	20	1	0	0	0	0	1	1	0	OFF	ON	ON	-1Vdc	-28V
	21	0	1	0	0	0	1	1	0	ON	OFF	ON	-2Vdc	-56V
	22	1	1	0	0	0	1	1	0	OFF	OFF	ON	-3Vdc	-84V
	23	0	0	0	1	0	1	1	0	ON	OFF	OFF	-4Vdc	-112V
	24	0	0	1	0	0	1	1	0	ON	ON	OFF	-5Vdc	-140V
	25	1	0	1	0	0	1	1	0	OFF	ON	OFF	-6Vdc	-168V
	26	0	1	1	0	0	1	1	0	ON	OFF	OFF	-7Vdc	-196V
	27	1	1	1	0	0	1	1	0	OFF	OFF	OFF	-8Vdc	-224V
	28	0	1	1	0	0	1	1	0	ON	OFF	OFF	-7Vdc	-196V
	29	1	0	1	0	0	1	1	0	OFF	ON	OFF	-6Vdc	-168V
	30	0	0	1	0	0	1	1	0	ON	ON	OFF	-5Vdc	-140V
	31	0	0	0	1	0	1	1	0	ON	OFF	OFF	-4Vdc	-112V
	32	1	1	0	0	0	1	1	0	OFF	OFF	ON	-3Vdc	-84V
	33	0	1	0	0	0	1	1	0	ON	OFF	ON	-2Vdc	-56V
	34	1	0	0	0	0	1	1	0	OFF	ON	ON	-1Vdc	-28V
	35	0	0	0	0	1	1	1	1	OFF	OFF	OFF	0Vdc	0V

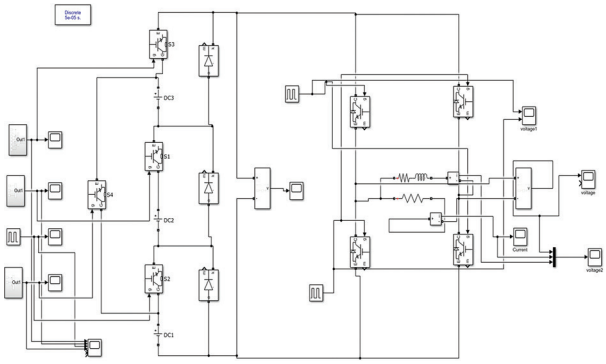

Fig. 7. Simulation Model of NRSCMLI

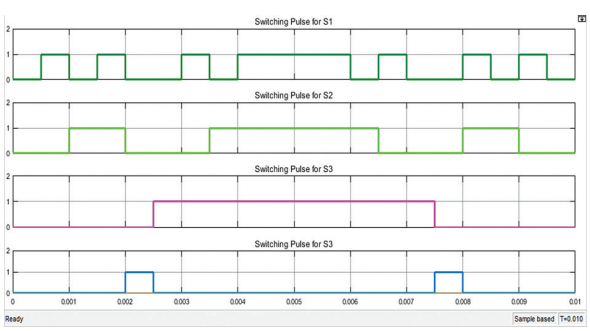

Fig. 8. Switching Pulses of NRSCMLI

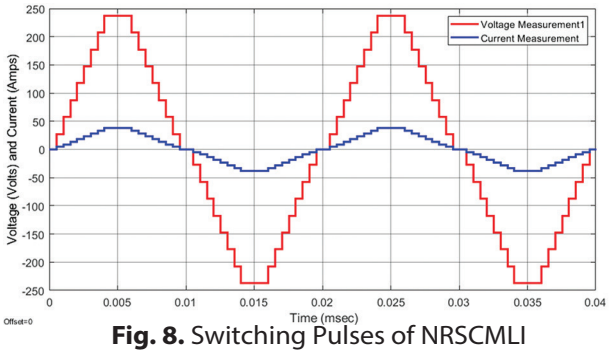

Fig. 8. Switching Pulses of NRSCMLI

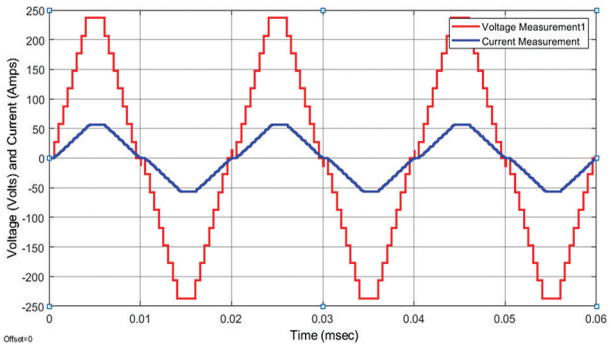

Fig. 9. 17-level output voltage and current of NRSCMLI for R load

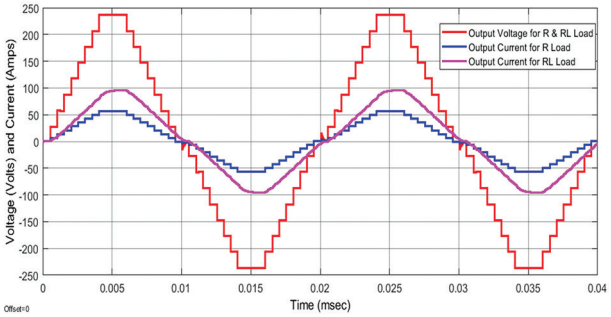

Fig. 11. Output voltage and current of NRSCMLI for parallel R and RL Load

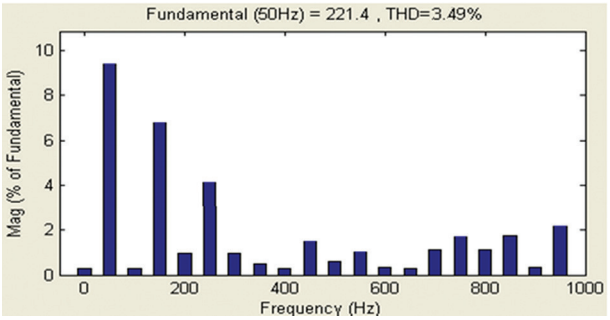

Fig. 12. FFT analysis

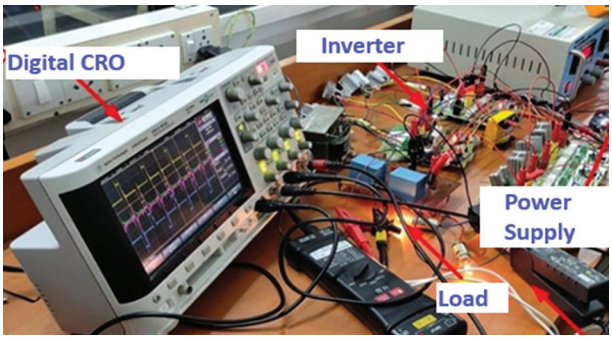

Fig. 13. Hardware output voltage waveform of new reduced switch count MLI

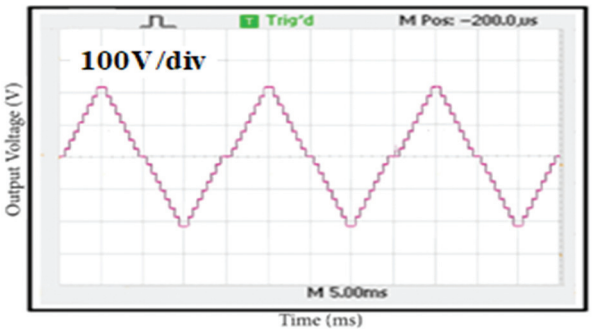

Fig. 14. Hardware output voltage waveform of new reduced switch count MLI

The microcontroller's control signal controls the MOSFET gate terminal's on and off states. Fig. 13 illustrates the hardware arrangement for the suggested NRSCMLI. Fig. 14 exhibits the hardware output voltage of the projected NRSCMLI. The output is measured for a resistive load of 1 kW. The hardware output current waveform is shown in Fig. 15. The magnitude of the load current is 2A and it is evident that the waveforms of the voltage and current are almost sinusoidal. Seventeen level MLI produces an output voltage of 224 volts at a frequency of 50 Hz. The efficiency was estimated using data from a MOSFET switch with variable output power. FFT analysis from Fig. 16 displays that the voltage THD is 3.51%.

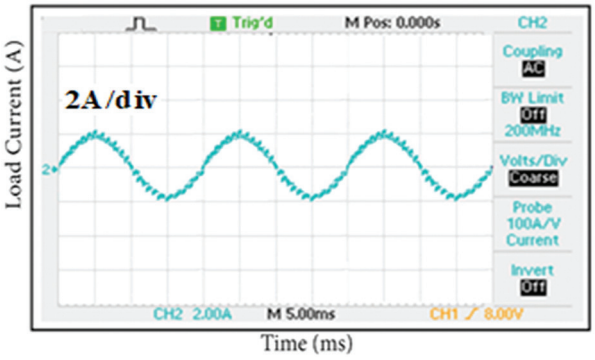

Fig. 15. Hardware output current waveform of new reduced switch count MLI

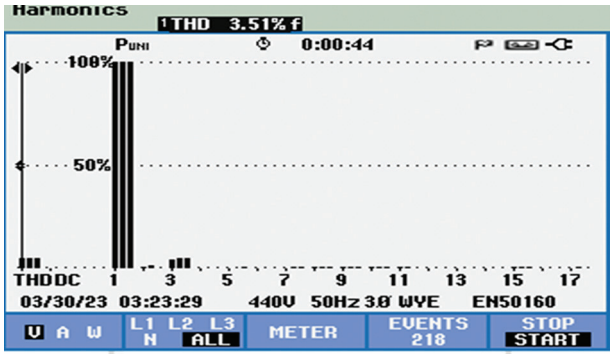

Fig. 16. Hardware FFT analysis of 17-level new reduced switch count MLI

7. CALCULATION OF TSV AND COST FUNCTION

From Fig. 1, components of conventional MLIs are calculated. Total standing voltage and cost functions for the MLIs are calculated as follows:

$$\text{Total Standing Voltage} = \sum_{i=1}^{n} MBV_{Si} \quad (14)$$

$$CF = (N_S + N_{gd} + N_D + N_C + \alpha TSV_{PU}) \times N_{DC} \quad (15)$$

N_S – Number of Switches
N_{gd} – Number of gate drives
N_D – Number of Diodes
N_C – Number of Capacitors
TSV – Total Standing Voltage
α – Weight co-efficient
N_{DC} – Number of Sources

7.1. DIODE CLAMPED MLI (DCMLI)

N_S=N_{gd}=16, N_D=14, N_C=8, α=1, N_{DC}=1& TSV_{PU} is 32
Cost Function = (16+16+14+8+32)*1= 86
CF/Level = CF/(Number of Levels) = 5.1

7.2. FLYING CAPACITOR MLI (FCMLI)

N_S=N_{gd}=16, N_D=0, N_C=18, α=1, N_{DC}=1 & TSV_{PU} is 32

Cost Function = (16+16+0+18+32)*1= 82

CF/Level = CF/(Number of Levels) = 4.8

7.3. CASCADED H-BRIDGE MLI (CHBMLI)

N_S=N_{gd}=32, N_D=N_C=0, α=1, N_{DC}=8 & TSV_{PU} is 4

Cost Function = (32+32+0+0+4)*8= 544

CF/Level = CF/(Number of Levels) = 32

7.4. CASCADED H-BRIDGE HYBRID MLI (CHBHMLI)

N_S=N_{gd}=12, N_D=N_C=0, α=1, N_{DC}=3 & TSV_{PU} is 6

Cost Function = (12+12+0+0+6)*3= 90

CF/Level = CF/(Number of Levels) = 5.3

7.5. NEW CASCADED MLI (NCMLI)

N_S=20, N_{gd}=18, N_D=N_C=0, α=1, N_{DC}=8 & TSV_{PU} is 11

Cost Function = (20+18+0+0+6)*8= 392

CF/Level = CF/(Number of Levels) = 23.1

7.6. NEW CASCADED HYBRID MLI (NCHMLI)

N_S=12, N_{gd}=10, N_D=N_C=0, α=1, N_{DC}=4 & TSV_{PU} is 8.25

Cost Function = (12+10+0+0+8.25)*4= 121

CF/Level = CF/(Number of Levels) = 7.1

7.7. MODIFIED CASCADED MLI (MCMLI)

N_S=12, N_{gd}=10, N_D=N_C=0, α=1, N_{DC}=4 & TSV_{PU} is 8.25

Cost Function = (12+10+0+0+8.25)*4= 121

CF/Level = CF/(Number of Levels) = 7.1

7.8. MODIFIED HYBRID MLI (MCMLI)

N_S=8, N_{gd}=6, N_D=4, N_C=0, α=1, N_{DC}=4 & TSV_{PU} is 6.12

Cost Function = (8+6+4+0+6.12)*4= 96.5

CF/Level = CF/(Number of Levels) = 5.7

7.9. PROPOSED MLI

Total standing voltage and cost functions for the proposed MLI are calculated as follows:

$TSV = MBV_{S1}+MBV_{S2}+MBV_{S3}+MBV_{S4}+MBV_{S5}+MBV_{S6}+MBV_{S7}+MBV_{S8}$

TSV=3.5V_{dc}+4V_{dc}+2.5V_{dc}+3.5V_{dc}+4V_{dc}+4V_{dc}+4V_{dc}+4V_{dc} = 29.5V_{dc}

$TSV_{PU} = TSV/MBV$ = (29.5V_{dc})/(8V_{dc})=3.6875

N_S =8, N_{gd} = 6, N_D = 3, N_C =0, α =1 and N_{DC} = 3

CF=(8+6+3+0+1×3.6875)×3= 62.0625

CF/Level = CF/(Number of Levels) = 62.0625/17=3.65

From the above calculations, the cost function per level is lower when compared to conventional topologies. So, it can be easily configured as three phase system with 24 switches, 20 driver circuits, 9 DC sources, and 9 diodes.

8. PERFORMANCE COMPARISON OF MULTILEVEL INVERTERS

The several MLI structures are compared to stages associated with the quantity of power switches employed. Table 2 shows the comparison of various types of MLIs based on the needs of switches, driver circuits, diodes, capacitors, and DC sources. TBVpu, cost function per unit and THD are also compared. Fig. 17 represents the pictorial representations of the comparison of various existing MLIs. Figure 18 depicts the comparison of the efficiency of various existing MLIs, it is clear that the suggested topology produces 98.60%. The NRSCMLI has benefits of 17 level with only 8 power switches when multisource is utilized; THD is 3.51% and efficiency is also high when compared to various multilevel inverters. The proposed MLI 3 DC sources are used to generate 17-levels output, whereas in conventional inverters, a minimum of 4 DC sources are required; otherwise, one or two sources with more capacitors are required to generate the same 17-level output. With the use of more capacitors, voltage balancing issues may arise. From the comparison, it appears that the developed MLI is best suited for electric vehicle applications with low power switches, reduced THD, and more efficiency.

Table 2. Performance Comparison of Multilevel Inverters

S.No.	Name of the Topology	Switches Needed	Driver Circuits Needed	Diodes Needed	Capacitors Needed	DC Sources Needed	TBV_{pu}	CF α=0.5	CF α=1	THD	Efficiency (%)
1	DCMLI	16	16	14	8	1	32	4.1	5.1	7.53	96.81
2	FCMLI	16	16	0	18	1	32	3.9	4.8	7.12	96.52
3	CHBMLI	32	32	0	0	8	4	31.1	32	7.81	95.75
4	CHBHMLI	12	12	0	0	3	6	4.8	5.3	7.1	97.10
5	NCMLI	20	18	0	0	8	11	20.5	23.1	7.44	96.21
6	NCHMLI	12	10	0	0	4	8.25	6.1	7.1	5.51	97.12
7	MCMLI	12	10	8	0	8	7.5	15.9	17.6	6.26	96.88
8	MHMLI	8	6	4	0	4	6.12	5.0	5.7	4.71	98.24
9	Proposed MLI	8	6	3	0	3	3.68	3.3	3.6	3.49	98.60

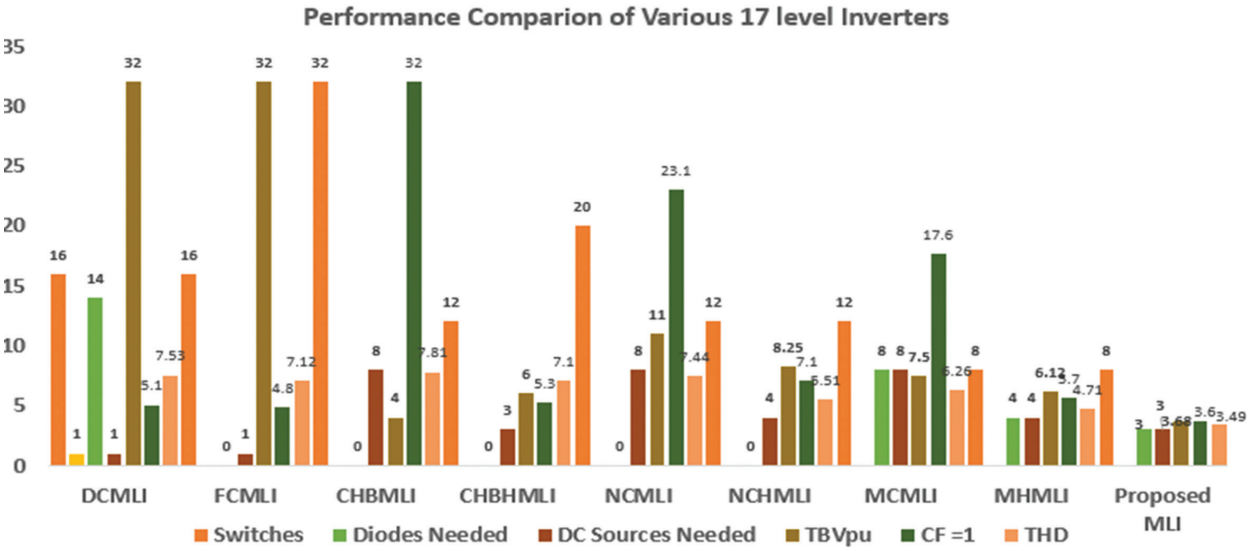

Fig. 17. Performance Comparison of various existing 17 level inverters

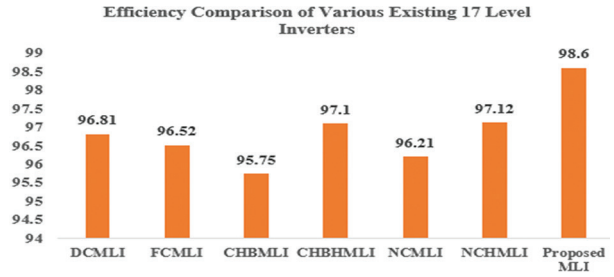

Fig. 18. Comparison of Efficiency of various MLIs

9. CONCLUSION

The proposed work has been validated on the fundamental structural set-up of the new reduced switch count MLI for electric vehicle applications. The different MLI structures and their circuit operations have been discussed. The mathematical expressions for the calculation of the needed voltage magnitude at the load have been pronounced. In the conservative approach, as the levels increase, the essential power switches also increase. Due to the large count of power switches, the harmonics, total harmonic distortion, switching losses, and implementation costs have also increased. The suggested topology considerably reduces the power switches to 8 for 17 levels, which lowers the losses due to reduced switching and conduction losses and improves the efficiency to 98.60%. The cost function is 3.6 for a weight coefficient of 1. Lower-order harmonics are removed, which leads to an improvement in reduced total harmonic distortion (THD) of 3.49%. Hence, the developed MLI is best suited for electric vehicle applications.

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