Area and Power Optimized Architecture of Sample Rate Converter for IoT Gateway Applications

Original Scientific Paper

Swetha Pinjerla*
Department of ECE, Jawaharlal Nehru Technological University,
Hyderabad, India
pswetha0823@gmail.com

Surampudi Srinivasa Rao
Department of ECE, Muffakham Jah College of Engineering and Technology,
Hyderabad, India
ssrao.atri@gmail.com

Puttha Chandrasekhar Reddy
Department of ECE, Jawaharlal Nehru Technological University,
Hyderabad, India
drpcsreddy@gmail.com

*Corresponding author

Abstract *– Nowadays, the Internet of things plays a major role in society for various applications such as medical diagnostics, telecommunications, agriculture, mobile computing, broadcasting, video surveillance etc. In Internet of Things (IoT) networks, several sensors with different data rates should be integrated to perform overall control or monitoring processes.High-speed data transmission technologies should be needed to communicate with IoT servers or storage. Generally, a gateway device is used to integrate low-data rate devices and IoT interfaces. Field Programmable Gate Array Logic (FPGA) can be utilized to implement high-speed and low-power gateway. The paper suggests a design of an FPGA-based IoT gateway architecture, which allows multi-protocol communications and an effective way of controlling sample rates. The design provides RF transceivers, protocol specific modules, and dynamic Sample Rate (SR) Selector to support smooth synchronization of data between diverse IoT devices. Clock generation and control blocks guarantee adaptive frequency assignment and upsampling and downsampling CIC filtering-based units ensure good signal conditioning. Experimental analysis shows that the presented method creates the low root mean square error (RMSE): 1.2 percent (downlink) and 1.4 percent (uplink), and high signal to noise ratios (SNR): 26.3 dB (downlink) and 24.8 dB (uplink) in 45 nm CMOS technology, resulting in better results than conventional 180 nm implementations. The Application-Specific Integrated Circuit (ASIC) implementation achieved a compact core area, reducing from 2.3 μm² at 180 nm to 0.3 μm² at 45 nm, demonstrating significant area efficiency with technology scaling. The results affirm that the architecture can provide reliable and high-quality data transfers of next-generation IoT gateways.*

Keywords: *Internet of things, Sample Rate Converter, Digital Gateway, IoT interface, Field Programmable Gate Array Logic, Xilinx FPGA*

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1. INTRODUCTION

FPGAs function as cost-effective integrated tools used in communication systems and various other application domains that continue to evolve. Software Defined Radio (SDR) systems employing FPGAs for hardware acceleration provide processors with extensive capabilities for deploying waveforms that promise both reconfigurability and portability.

A sampling rate conversion system contains the decimation filter (decimator) which serves as its foundational element. The decimation filter executes both low-pass filtering together with down-sampling operations. The filter changes high-frequency high-bit-rate low-resolution data into low-frequency high-resolution data. The system finds its primary applications in the areas of speech processing as well as radar antenna and communication systems. In recent years, researchers have actively worked on devel-

oping decimation filters with enhanced performance. Decimation depends on both a high-quality low-pass filter and a sampling rate converter to perform frequency reduction of the sampling data [1].

The changing of sampling rates for processed digital signals becomes vital or practical in numerous signal processing applications. The actual task proves simple for most cases yet high-ratio interpolation and decimation operations need digital low-pass filters to maintain small bandwidth areas along with narrow transition bands. When filter requirements include long impulse response duration it leads to very complex implementations for both interpolation and decimation algorithms. A solution to Frequency Response Masking (FRM) involves splitting the resampling filter design into separate filters with more achievable specifications. The implementation complexity decreases when non-zero coefficients are reduced across the entire filter structure in the design results [2].

Telecommunication businesses adopt Digital Down Converter (DDC) technology as their primary tool. Suppliers select DDC converters as a standard component for cellular phones. A cell phone chip contains variable frequency amplifiers together with high-speed (12 or 14 bits) Analog-to-Digital converters and DDC. Design operating specifications of the parts range from 50 MHz to 65 MHz with oscillations enabling usage of Signal parts at frequencies up to 300 MHz. DDC enables users to program the frequency together with bandwidth settings during data conversion operations. The conversion operation together with filtering takes place digitally through a linear sequence. The combination of DDC and a digital I / Q demodulator functions with frequency programmability [3]. Fixed-ratio multi-rate techniques using L/M, where both are positive integers, serve as standard sample rate conversion (SRC) methods.The B-spline interpolation performs the conversion process to change the sample rate. The approach enables the completion of Digital Audio Tape (DAT) to Compact Disc (CD) sample rate conversion while all CD-to-DAT filter coefficients remain unaffected. Hogenauer filters operate as cascaded integrated comb filters for digital systems to deliver major alterations in sampling rates [4].

The processing requirement for sample rate conversion is high while channelisation takes place in this stage. A bandlimited Intermediate Frequency (IF) digital signal processed at a high sampling rate obtains its low-frequency components by mixing it with digital oscillator samples in a quadrature position. After down-conversion, the signal gets decimated to its required sampling rate with subsequent filtering done to it. Paul Burns shows that each channel requires two expensive high-end Digital signal processors (DSPs) during the down-conversion operation. Reconfigurable FPGAs replace Digital signal processors while providing high-skill design options together with accurate computational power and better performance execution [5].

The proposed work introduces an optimized IoT gateway architecture that integrates multiple low-data-rate communication protocols (LoRa, Sigfox, and NarrowBand-Internet of Things (NB-IoT)) with a high-speed Wi-Fi interface using FPGA-based implementation. The core novelty lies in the design of an efficient sample rate conversion strategy, where cascaded CIC filters are employed for both interpolation and decimation processes. To further minimize distortion, the interpolation unit incorporates CIC filtering followed by D flip-flops and an averaging circuit, while the downsampling path integrates D flip-flops before the CIC stage to produce a smooth signal. The proposed architecture is optimized for reduced hardware resource utilization and low power consumption, making it suitable for energy-constrained IoT applications.

The main contributions of this work can be summarized as follows:

- A unified hardware architecture that supports multiple IoT protocols on the sensor side and Wi-Fi on the IoT server side.
- Introduction of cascaded CIC filters with auxiliary circuits (DFFs and averaging units) to reduce high-frequency distortions during upsampling and downsampling.
- Development of a multi-frequency clock generation mechanism using sequential counters and flip-flops to achieve flexible protocol switching with low area overhead.
- The architecture is tailored to minimize slice LUTs, registers, and flip-flops while reducing dynamic and static power consumption on FPGA and the proposed system achieves enhanced reconstruction quality, validated through RMSE and SNR analysis.

2. LITERATURE SURVEY

A review of significant research findings explores modern architectural and methodological strategies which enhance performance for SDR and electronic warfare and real-time data acquisition systems.

The power of the multichannel fractional sample rate convertor could be reduced through the optimization of filter coefficient hamming distance by using Genetic algorithms according to Vivek's proposal. The key element of the multichannel fractional sample rate convertor consists of the Cascaded multiple architecture finite impulse response filter (CMFIR filter). The CMFIR filter works through the successive implementation of CIC & multiply-accumulate architecture (MAC) FIR filter components. The genetic algorithm minimizes how well-matched successive filter coefficients of the CMFIR filter are to each other in terms of the Hamming distance.The reduction of the hamming distance between filter coefficients leads to reduced transitions between the values of 0 and 1 or 1 and 0. The methods minimize both Complementary Metal-Oxide-Semiconductor (CMOS) transistor switching and therefore decrease total Dynamic power usage in multichannel sample rate converters [6]. Brunel et al

developed an FPGA circuit for Software Defined Radio applications which executes arbitrary-ratio signal re-sampling between the Low-Frequency band and Very High-Frequency ranges. This SDR application allows designers to manage Spurious-Free Dynamic Range (SFDR) with an easy implementation that functions independently of additional clock requirements which suits FPGA designs with limited clock resources [7]. The architecture proposed by Debarshi et al. consists of a COordinate Rotation Digital Computer (CORDIC) processor as a digital oscillator before a multi-stage CIC filter which acts as a high-rate decimation filter. An MSFIR decimation filter with multiple output channels performs perfect results through its design. Design and implementation of the entire proposed DDC architecture occurred in the Xilinx ISE 14.7 simulator through optimization techniques targeted to operate on a Xilinx Kintex-7 FPGA device. Implementing DDC on FPGA offers high flexibility, moderate cost, and customizable design options [8].

Xinxing et al. put forward an optimization design method which implements parallel digital down-conversion combined with polyphase filtering. The mathematical model of high-speed digital down-conversion starts with derivation followed by an efficient implementation design of traditional DDC architecture. A down-conversion structure for high-speed frequencies has been designed through parallel filtering and frequency conversion. The paper provides instructions for two main design aspects of parallel frequency conversion parameters and multipath filter coefficient calculation methods [9]. The acquisition system designed by Dai et al incorporates a 5Gsps real-time sampling rate together with PXI bus-based mass storage. A system sampler achieves parallel sampling through its multi-core analog-to-digital converter (ADC). The system features an exact sampling timer along with sufficient digital values that support real-time sampling performances. FPGA technology serves as the solution to acquire fast data samples from the ADC.The serial-to-parallel module in the FPGA reduces the data rate. The trigger detection unit functions to manage storage procedures to increase detection capabilities for short-duration signals. The system gains improved capability to acquire high-speed signals because of its designed mass data storage structure [10].

Xiang et al. details an FPGA based analog to digital converter implementation tailored for extreme cryogenic conditions (liquid helium). They propose a soft-core, multi-lane ADC architecture—likely implying parallel digitization channels implemented as FPGA IP—to function robustly at extremely low temperatures. This work is significant because typical ADC hardware fails in cryogenic environments, and soft-core logic on FPGA provides flexibility and resilience. Applications could include quantum computing sensors or space-based cryogenic instrumentation [11]. Agarwal and Bopanna presents a reconfigurable pipelined architecture for a sample-rate conversion (SRC) filter, optimized for software-defined radio (SDR) receivers. Utilization of pipelining suggests a focus on high throughput and timing efficiency. The architecture likely supports dynamic reconfiguration, enabling different sample rates on-the-fly in SDR contexts, improving flexibility and performance under changing operational conditions [12]. Liu et al. introduces an FPGA design that executes 1024-channel channelization—dividing an input wideband signal into 1024 narrower sub-bands—for SDR applications. The architecture is reconfigurable, enabling adjustments to channel characteristics (like bandwidth or center frequency). This is particularly relevant for high-density SDR systems and spectral processing, such as cognitive radio or multiprotocol monitoring [13].

Zeineddine et al. propose an FPGA-based approach for arbitrary sample-rate conversion, facilitating multi-standard digital front-ends in one flexible architecture. This is key for devices that must handle diverse standards requiring different sampling rates. The focus is on efficiency—both in resource use and performance—supporting seamless interoperability among multiple RF standards [14]. Agarwal and Bopanna et al. describes a multi-rate filtering architecture for SDR receivers utilizing distributed arithmetic (DA). DA allows multiplierless implementation, saving FPGA logic, and offers low-latency, area-efficient performance, which is critical in real-time SDR applications. The multi-rate capability indicates adaptability to different sampling frequencies or standards [15].

Different effective approaches in multichannel sample rate conversion and digital down-conversion and high-speed data acquisition surface through the reviewed studies. Multichannel sample rate conversion systems achieve increased power efficiency and computational performance through Genetic Algorithms alongside FPGA-based architectures and parallel processing methods. The incorporation of modern filter structures with re-sampling protocols boosted SDR and electronic warfare system capabilities. Data processing together with storage at high speeds turns out to be highly effective when implemented using FPGA-based acquisition systems.The developed innovations create a solid basis which researchers can use to establish improved digital signal processing technologies that utilize resources efficiently at scale.

3. AREA AND POWER OPTIMIZED ARCHITECTURE OF SAMPLE RATE CONVERTER FOR IOT GATEWAY APPLICATIONS

3.1. IOT GATEWAY

The fast expansion of the IoT demands the incorporation of heterogeneous devices and communications protocols that have different power and networking capacities. The IoT gateways have thus become a very important element, allowing smooth connectivity and offering the computing power required in an edge computing environment. A home Internet Gateway links the Local Area Network (LAN) to the Internet Service

Provider network [16]. The IoT devices establish connections to the IoT Gateway through various wireless protocols that include Sub-Gigahertz (Sub-GHz), Long Range Wide Area Network (LoRaWAN), Sigfox, Long-Term Evolution (LTE), LTE-Machine Type Communication (LTE-M), and Wi-Fi. The system establishes Internet connectivity (Public Cloud) through either Ethernet LAN or Fiber Optics Wide Area Network (WAN) network connections. The connection between IoT devices and IoT Gateway and connected IoT systems as illustrated in Fig. 1 [17].

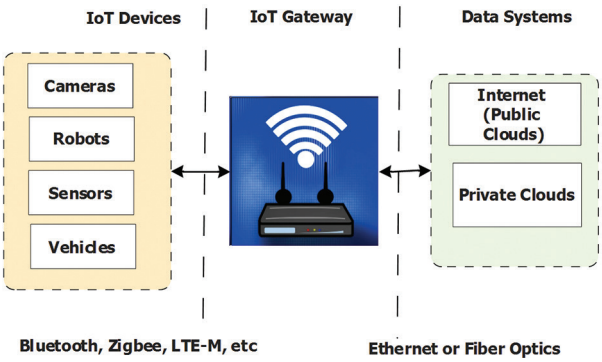

Fig. 1. Interface with IoT devices, IoT Gateway and, IoT systems

3.2. LORA

LoRa is a low-power wide-area network (LPWAN) modulation technology developed by Semtech, designed for long-range connectivity with minimal energy consumption. It enables communication up to 3 miles (5 km) in urban areas and over 10 miles (15 km) in rural environments. LoRaWAN, the networking standard built on LoRa, employs a star topology to connect large numbers of low-power devices requiring deep indoor or wide-area coverage [18].

3.3. SIGFOX

Sigfox is an ultra-narrowband low-power wide area network (LPWAN) technology that supports Binary Phase-Shift Keying (BPSK) modulation to transport data on unlicensed bands of the radio spectrum, including the 915 MHz ISM band in the US. Its end point radios are simple and make the devices low cost and low powered, whereas the communication is handled by complex base stations. Sigfox can transmit very low data rates, up to 300 baud, with small 12 bytes of payload per message. The uplink communication is mainly based on DBPSK and downlink on GFSK. Its long range low power transmission makes it applicable in smart metering and remote sensing, although the limited bandwidth is a disadvantage [19].

3.4. NBIOT

NB-IoT is an LPWAN based on standards that can support large-scale IoT deployments with improved power efficiency, capacity, and spectrum use. It enables deep indoor and rural coverage with ultra-low device complexity, enabling battery life of more than a decade. NB-IoT module is affordable, similar to Global System for Mobile Communications / General Packet Radio Service (GSM/GPRS) modules, and has the advantages of lower manufacturing costs the more it is adopted [20].

3.5. PROPOSED FPGA ARCHITECTURE

Fig. 2 shows the proposed FPGA-based architecture of an IoT gateway that enables multi-protocol communication and an efficient SRC. The RF transceivers have been used at the top and bottom of the framework to support the wireless communication interfaces that allow two-way data traffic between the IoT sensor nodes and the central gateway. The FPGA has a number of dedicated modules that work in unison to provide smooth protocol integration and data synchronization, as well as optimization of sample rates. The Wi-Fi interface provides high-speed access to IoT servers and storage and is the main data upload and downstream control channel.

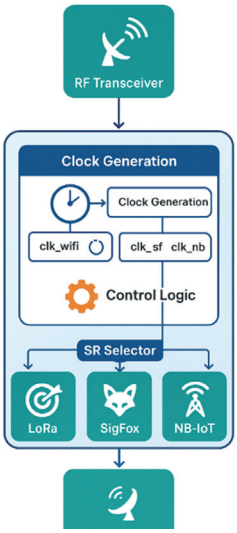

Fig. 2. Proposed Architecture

There is a special clock generation unit which generates numerous synchronised clock signals- such as clk_{WiFi} , clk_{sf}, clk_{nb}, and clk_{lora} which are in line with various wireless standards. A clock control block manages these clock signals and enables the flexibility and adaptive frequency assignment to various sensor protocols. The design can be considered as a central module, the Sample Rate (SR) Selector that enables a dynamic switch between different IoT communication protocols such as LoRa, Sigfox, and NB-IoT. All these communication blocks contain upsampling (U) and downsampling (D) blocks, which are also realized with CIC filters and allow interpolation and decimation. The upsamplers condition the low-data-rate sensor signals before they are transmitted and the downsamplers condition the high-data-rate incoming signals to be compatible with the storage and control interfaces. Such a configuration makes it possible to effectively synchronize and transfer data using heterogeneous devices without quality loss.

Fig. 3 has shown the block diagram of the proposed IoT Gateway that is capable of integrating various communication protocols by the centralized processing core that is based on FPGA. The architecture is aimed at easing the exchange of heterogeneous IoT devices with the internet infrastructure. On the front end, the Input RF Interface receives incoming wireless signals of IoT nodes with a wide range of protocols including NB-IoT, SigFox, and LoRa. These signals are then fed into an FPGA, where they are processed in a manner that includes protocol translation, data synchronization and filtering so that they are compatible with the system. The Output RF Interface is responsible on the transmission side to deliver processed data back to the IoT devices or IoT networks to which it is connected. The system also includes the Wi-Fi module to offer high-speed backhaul connection to cloud platforms or local servers to store, analyze and monitor. The design will be interoperable across a large range of IoT devices by incorporating NB-IoT, SigFox, and LoRa within the gateway, using those different frequency bands and communication protocols. The FPGA is the central controller, which coordinates protocol, switching, and real-time processing, and thus, the low-latency communication, scalability, and adaptability.

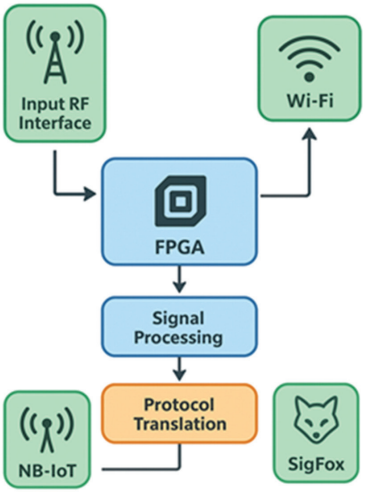

Fig. 3. IoT Gateway Block

3.6. CIC FILTER

The CIC digital filters represent a cost-effective method to implement narrowband low-pass filters that find applications in hardware solutions for decimation and interpolation functions and delta-sigma converter filtering. CIC filters excel in anti-aliasing functions during sample rate reduction operations as well as anti-imaging applications in signal sample rate increase scenarios. The applications require fast data processing which includes hardware quadrature modulation and demodulation for wireless systems as well as delta-sigma A/D and D/A converters. Tapped-delay line finite impulse response (FIR) filters with linear-phase work to fix the non-flat passband characteristics of CIC filters by following them or placing them before them.The cascaded-filter architectures have valuable benefits.

- The FIR filters operate at reduced clock rates minimizing power consumption in high-speed hardware applications
- CIC filters are popular in hardware devices; they need no filter coefficient data storage and require no multiplications. The arithmetic needed to implement CIC filters is strictly additions and subtractions only.
- Narrowband low-pass filtering can be attained at a greatly reduced computational complexity compared to using a single low-pass FIR filter. This property is why CIC filters are so attractive in decimating and interpolating DSP systems.

CIC filters structure the comb section either before or after their integrator section. Placing the comb section into the filter running at the lower sample rate demonstrates practical sense. The typical method of implementing CIC filters occurs when comb filters exchange positions with down-sampling operations. The world received CIC filters from Hogenauer in 1981 along with this fundamental characteristic. The comb component of the decimation filter shows a shorter delay length (differential delay) equal to $N = D/R$. The equivalent comb delay relationship exists between post-downsampling by R results in N samples but pre-downsampling by R produces D samples. Similarly, the comb delay between premultiplication by R with N samples provides the same result as post-sampling by R with D samples. The new configuration leads to two essential advantages that enable data storage reduction through $N = D/R$ differential delay line shortening as well as reduced clock frequency operation.The implementation shortens hardware power consumption through these two effects. Fig. 4 shows the interpolator using a CIC filter. Fig. 5 shows the decimated using the CIC filter.

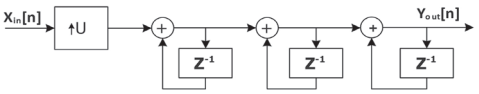

Fig. 4. Interpolator using CIC filter

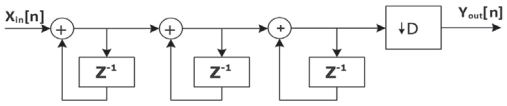

Fig. 5. Decimator using CIC filter

3.7. CIC FILTER BASED DOWN SAMPLER AND UPSAMPLER

Fig. 6. displays the sample rate converter with Interpolator and Decimater CIC filter. The architecture uses CIC filters with rate converters to do both interpolation and decimation operations. The CIC filter is applied to the incoming signal in the forward path and this helps reduce aliasing and spectral distortion before it is relayed to the rate converter where the sampling frequency is adjusted based on system needs. The filter control unit synchronizes the CIC filter functions, and provides adaptive filtering in both the upsampling and downsampling operations.

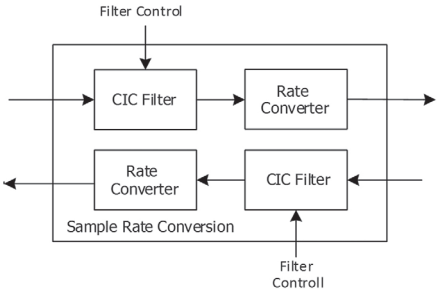

Fig. 6. Sample rate converter using Interpolator and Decimater with CIC filter

4. RESULT AND DISCUSSION

The proposed design is coded using Verilog HDL. The design is synthesized using Xilinx Vivado software. The system is implemented using Xilinx Virtex-4 FPGA device.The synthesis process is performed in a Windows 11 system with 6GB RAM @ 2.4 GHz operating frequency. The proposed design is synthesized in 180n and 45nm technology using cadence genus tools to evaluate the power and delay performance. Fig. 7 shows the simulated output using Modelsim.

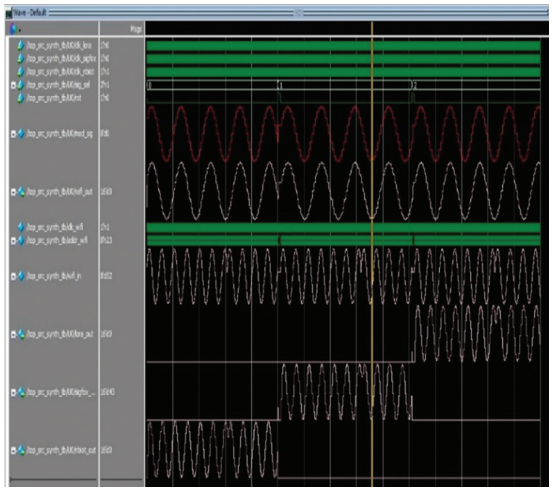

Fig. 7. Simulated output using Modelsim

Signal-to-Noise Ratio

SNR functions as a quality measure which indicates the potential for false switching through a basic estimation of implementation performance comparison as shown in Equation (1).

$$SNR = \frac{V_{sig}}{\sqrt{\sum_i^N V_n^2}} \quad (1)$$

V_1, V_2 … VN are noise sources which can be signal dependent, like the shot noise or signal independently.

Root Mean-Square Error

The RMSE of the estimated signal $\hat{x}(n)$ for M simulation, runs are calculated by Equation (2).

$$RMSE = \sqrt{\frac{1}{M}\sum_{j=1}^{M}\frac{1}{N}\sum_{n=1}^{N}(y(n) - \hat{x}_{hk}^{[j]}(n))^2} \quad (2)$$

4.1. FPGA PERFORMANCE EVALUATION

Table 1 shows the individual module resource utilization. Table 2 presents a comparison of resource utilization between the proposed design and previously reported techniques. The results show that the proposed work requires significantly fewer registers (193), LUTs (246), and IOBs (70), highlighting its efficiency over existing methods.

Table 1. Individual Module Resource Utilization

Module Name	Slice LUTs (20,800)	Slice Registers (41,600)	Slices (81,650)	LUT as Logic (20,800)	Bonded IOBs (106)	BUFGCTRL (32)
top_src_synth	246	193	99	246	79	4
Uaddr (AddrGen)	84	24	27	84	0	0
Uclkdiv (ClockDiv)	2	1	2	2	0	0
Udec0 (Decimate)	40	20	20	40	0	0
Udec1 (Decimate_0)	40	19	19	40	0	0
Udec2 (Decimate_1)	40	20	20	40	0	0
Uint (Interpolate)	40	48	17	40	0	0

Table 2. Resource Utilization with Previous Techniques

Method	Number of Slice Registers	No. of LUT	No. of IOB	Number of Block RAM/FIFO	No. of DSP
[7]	560	298	-	-	26
[12]	24452	44724	-	-	-
[13]	46245	36995	-	170	-
[14]	4173	3275	-	-	-
This work	193	246	70	-	-

4.2. POWER PERFORMANCE

Table 3 shows the overall FPGA resource utilization, where LUTs (1.18%) and registers (0.46%) occupy a very small fraction of the available resources, while I/O usage is comparatively high at 74.53% due to external connectivity, and BUFG utilization remains moderate at 12.5%. Table 4 presents the power consumption analysis, indicating that dynamic power dominates at 99%, with I/O operations contributing the largest share (83%), while static power is minimal at only 1%. Fig.8 shows the overall Register–Transfer Level (RTL) schematic. Fig. 9 shows the implementation in Virtex-4 FPGA. Fig. 10. shows the RTL of the downconverter in the cadence genus tool. Fig. 11. shows the RTL of the Upconverter in the cadence genus tool. Fig. 12. shows the overall circuit in cadence genus tool.

Table 3. Overall Resource Utilization

Resource	Utilization	Available	Utilization %
LUT	246	20800	1.18%
FF	193	41600	0.46%
IO	79	106	74.53%
BUFG	4	32	12.50%

Table 4. Power consumption

Category	Sub-Category	Power (W)	Percentage
Dynamic (33.942 W, 99%)	Signals	3.129 W	9%
	Logic	2.667 W	8%
	I/O	28.147 W	83%
Static (0.485 W, 1%)	PL Static	0.485 W	100%

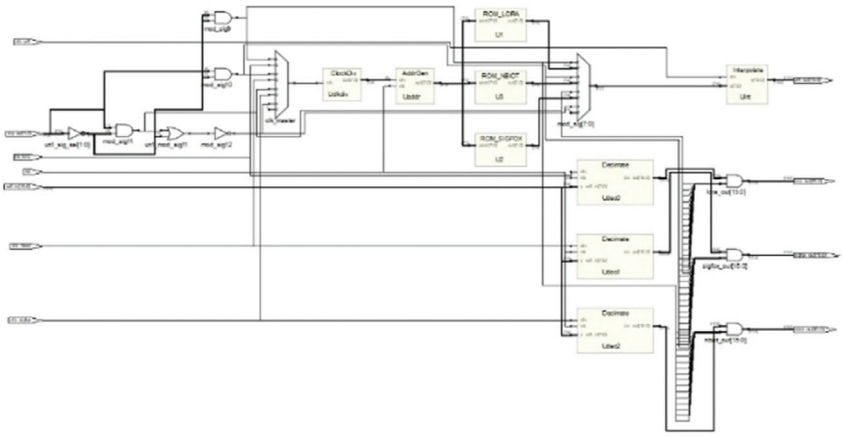

Fig. 8. Overall RTL schematic

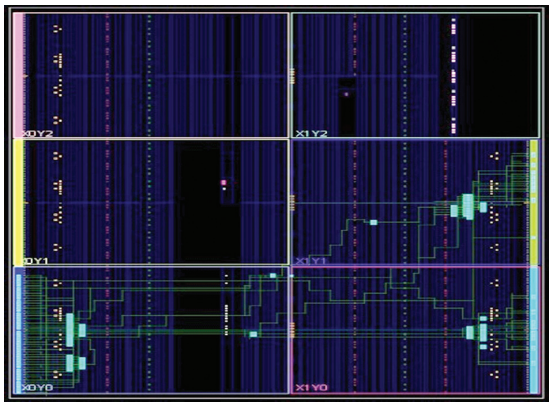

Fig. 9. Implemented in Virtex-4 FPGA

Table 5 presents the ASIC performance evaluation, where the proposed work achieves the lowest cell count (2701) with reduced power consumption (2 mW) and improved delay (1.02 ns) at 180 nm technology, demonstrating better efficiency compared to previous methods.

Table 5. ASIC Performance Evaluation

Methods	Number of Cells	Power (mW)	Delay (ns)	Technology
[5]	48362	3.63	2.11	45nm
[15]	3246748	2.491	8	90 nm CMOS
This work	2701	2	1.02	180nm

Table 6 shows the synthesized power output for 180 nm and 45 nm CMOS technologies, where scaling down to 45 nm reduces the number of cells and leakage power, while also lowering internal and net power compared to 180 nm, with switching power remaining nearly the same.

Table 6. Synthesised power output using 180 nm and 45 nm

Technology	Number of Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
180 nm CMOS	2701	200.86	1225371.81	799191.57	2024563.38
45 nm CMOS	2006	109.39	1135487.67	689714.31	2021369.14

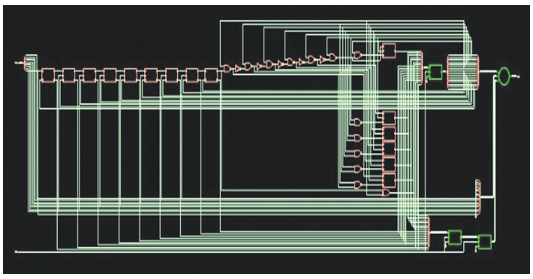

Fig. 10. RTL of downconverter in cadence genus tool

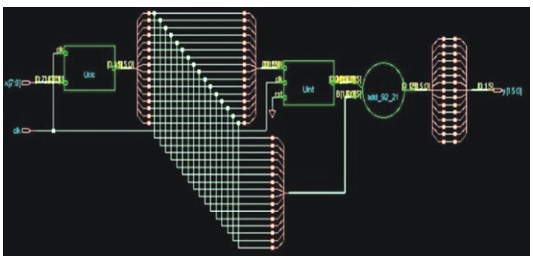

Fig. 11. RTL of Upconverter in cadence genus tool

Table 7 highlights the synthesized results for core area, showing that technology scaling from 180 nm to 45 nm significantly reduces the core area from 2.3 μm^2 to 0.3 μm^2, along with a decrease in the number of cells.

Table 7. Synthesized results for core area using 180nm and 45nm

Technology	Cells	Core Area(μm²)
180 nm CMOS	2701	2.3
45 nm CMOS	2006	0.3

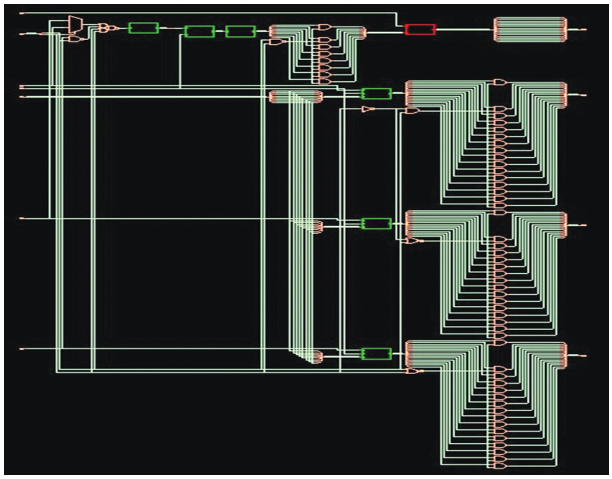

Fig. 12. Overall circuit in cadence genus tool

Table 8 compares RMSE and SNR across different technology nodes, showing that the 45 nm CMOS process achieves lower RMSE values (1.4% uplink, 1.2% downlink) and higher SNR (24.8 dB uplink, 26.3 dB downlink) compared to the 180 nm CMOS process, indicating superior signal quality and accuracy with scaling.

Table 8. Comparison of RMSE and SNR

Technology	Process (nm)	RMSE Uplink (%)	RMSE Downlink (%)	SNR Uplink (dB)	SNR Downlink (dB)
180 nm CMOS	180	3.2	2.8	18.5	20.1
45 nm CMOS	45	1.4	1.2	24.8	26.3

Table 9 provides a comparative evaluation of FPGA and ASIC implementations. The FPGA design shows very low logic utilization but high dynamic power consumption (33.94 W), while the ASIC implementations in 180 nm and 45 nm CMOS demonstrate significant improvements in power efficiency and area reduction, with the 45 nm technology achieving the most compact core area (0.3 μm²) and lowest leakage power.

Table 9. FPGA vs. ASIC Performance Comparison

Platform	Metric / Resource	Value
FPGA (Xilinx virtex-4)	LUT Utilization	246 / 20,800 (1.18%)
	FF (Registers)	193 / 41,600 (0.46%)
	IO	79 / 106 (74.53%)
	BUFG	4 / 32 (12.5%)
	Dynamic Power	33.942 W (99%)
	Static Power	0.485 W (1%)
	Total Power	34.427 W
	SNR / RMSE	63.4 dB / 0.0558
	Max Freq.	162.7 MHz
ASIC (180nm, 45nm)	Technology Node	180 nm CMOS
	Number of Cells	2,701
	Core Area	2.3 μm²
	Power Breakdown	Leakage: 200.86 nW Internal: 1,225,371.81 nW Net: 799,191.57 nW Switching: 2,024,563.38 nW
	Technology Node	45 nm CMOS
	Number of Cells	2,006
	Core Area	0.3 μm²
	Power Breakdown	Leakage: 109.39 nW Internal: 1,135,487.67 nW Net: 689,714.31 nW Switching: 2,021,369.14 nW

5. CONCLUSION

This work proposes a new area and power-optimized sample rate converter architecture for the IoT gate. Lora, SigFox and NbIoT protocols are used to generate low data rate input, and WiFi is used in the IoT storage interface side. A catch memory is used as the interface to receive the low data rate input and store it.The proposed work is implemented using Xilinx Virtex-4 FPGA and evaluated hardware resource utilization and power consumption performance.To evaluate hardware resource utilization, the number of slices, LUT, and flip flops are measured and compared with conventional implementation.This design achieved good performance regarding hardware resource utilization and power consumption. Experimental results demonstrate that the proposed method has low RMSE of 1.2% (downlink) and 1.4% (uplink), high SNR of 26.3 dB (downlink) and 24.8 dB (uplink) in 45 nm CMOS technology, which is better than conventional 180 nm implementations. Moreover, the ASIC implementation is also very area efficient, where the core area has been decreased by a factor of 8x between 180 nm (2.3 um 2) and 45 nm (0.3 um 2) due to the technology scaling. Future research directions will be aimed at the expansion of the proposed architecture to include acceptability of the latest 5G/6G IoT requirements, the machine learning-based traffic decision-making, and the energy efficient operation in ultra-low-power applications. In addition, the investigation of both reconfigurable hardware accelerators and security-aware integration of different protocols will contribute to the enlargement of the strength and deployment of the gateway in the big IoT environment.

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