Optimization Algorithms based compensation of mismatches in Time interleaved Analog to Digital Converters - A Review

Review Paper

Venkata naga chakravarthi Manepalli
Department of Electronics and Communication Engineering,
DR.Y.S.R. ANU College of Engineering and Technology,
Guntur, India-522510
chakrimvn@gmail.com

Chandramohan Bhuma
Department of Electronics and Communication Engineering, Bapatla Engineering College,
Bapatla, India-522101
chandrabhuma@gmail.com

Abstract *– Time interleaved analog to digital converters (TIADCs) play a significant role in signal processing wherever higher sampling rates are required. However, TIADCs suffer from various mismatches like sampling time, dc offset, gain, bandwidth etc. This results in generation of erroneous signal. Numerous methods were proposed for estimation of these mismatches and for correction of the erroneous signal. Optimization algorithms like genetic algorithm (GA), differential evolution (DE) algorithm were also used for estimation of mismatches. An overview of these algorithms and their performance comparison, with respect to various signal quality metrics like signal to noise ratio (SNR), signal to noise, distortion ratio (SNDR) etc, is given in this article.*

Keywords*: Time interleaved ADCs, mismatches, estimation, correction*

1. INTRODUCTION

Time interleaved analog to digital converters employ N parallel low rate ADCs which raise the overall sampling rate. In N-channel TIADCs a low rate channel of ADC operates with F_S/N sampling frequency. The block diagram of N-Channel TIADCs is shown in Fig.1. Each channel of TIADCs has a sampling time of NTs, and after reconstruction the overall system sampling time obtained is T_S. In the figure, $x(t)$ is the input applied to all ADCs and $y(nT)$ is the output after combining the outputs of low rate ADCs. However, the generated output is erroneous due to the mismatches existing in TIADCs. The most commonly occurring mismatches are gain, dc offset, sampling time and bandwidth mismatches. The mismatches among the channels' components result in generation of mismatch error in each channel. The mismatch error is dissimilar for different channels. The difference between the slope of ideal transfer characteristic and transfer characteristic with gain errors is known as gain mismatch. Similarly dc offset, bandwidth and timing mismatches are the differences in dc offsets, bandwidths and sampling times respectively.

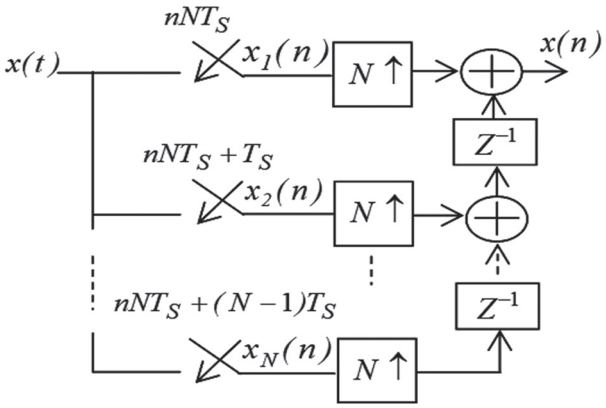


Fig. 1. N-Channel TIADCs

TIADCs with mismatches in sampling time, gain and dc offset is shown in Fig.2. Here T_i, Δg_i and Δx_i represent sampling time, gain and dc offset mismatches of i^{th} channel respectively. Various methods were suggested for reducing the effect of mismatches and to get compensated output. The output thus compensated has better SNDR (signal to noise and distortion ratio) and SFDR (spurious free dynamic range).

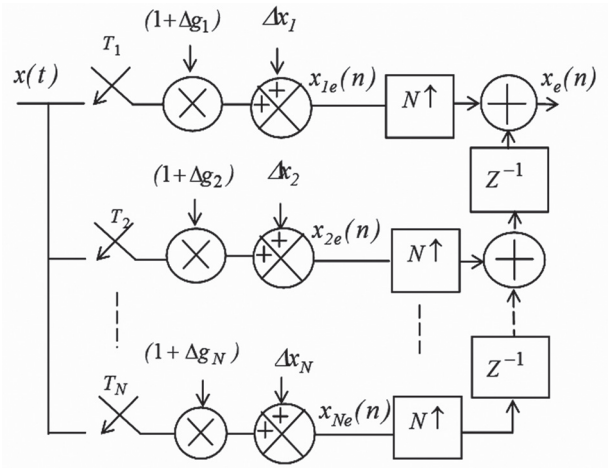


Fig. 2. TIADCs with mismatches

2. OPTIMIZATION ALGORITHMS USED FOR COMPENSATION OF MISMATCHES

Although there are numerous techniques existing for compensation of mismatches, the focus here is on optimization algorithms used for compensation. Optimization algorithms can be utilized to solve problems in fields like economics, sciences, engineering etc. Due to the growth of competition in all disciplines, the function of optimization has become still more prominent as the aim is to reduce the price of a product or wants to assign the resources wisely. The algorithms that are applied nowadays include genetic algorithm, differential evolution algorithm, ant colony optimization, particle swarm optimization, teacher-learner based optimization algorithm etc. Among of these algorithms, genetic and differential evolution algorithms were used for calibration of mismatches in TIADCs.

Differential evolution algorithm was applied for estimation of sampling time mismatch, dc offset and gain mismatches in 7 and 8-channel TIADCs in an OFDM system with 4-QPSK modulation. The method is evaluated by applying monotonic sinusoidal and image signals to the OFDM system [1]. Genetic algorithm based mismatch calibration was used for TIADCs with frequency dependent mismatches [2]. The sampling time mismatches were estimated by using modified differential evolution algorithm. An FPGA board was used to realize the algorithm and correction was applied in MATLAB [3].

A pilot signal was sent to train the neural network and then the sampled signals were directly calibrated with the trained network [4]. A differential evolution (DE) algorithm based estimation of sampling time mismatches was implemented [5]. Genetic Algorithm was used to estimate sampling time mismatches and fractional delay filters were used to correction [6]. A mean square algorithm was used to estimate the timing-error. The curve fitting algorithm was used to acquire the optimal sampling points and the best length of iterations [7]. Apart from these methods which used optimization algorithms, many other techniques were proposed which are summarized briefly below.

The first sub-ADC was chosen as a timing reference and first order Taylor approximation was used to estimate the errors in the samples due to the sampling time mismatches. Correction was applied by subtracting the error from erroneous samples [8]. Error estimation and calibration method using blind calibration technique was proposed to suppress the spurious components and restore the dynamic performance of sub-ADCs [9]. A digital background calibration method which makes use of Hadamard transform for calibrating gain, timing mismatches and dc offset mismatch cancellation by averaging was proposed [10]. Fast Fourier Transform Algorithm (FFT) based blind calibration algorithm was proposed for calibration of gain, offset and timing mismatches in a TIADC system with two channels [11]. Bandwidth mismatch optimization was performed using simulated annealing algorithm (SAA) [12]. The calibration of TIADCs and the challenges confronted by background calibration methods were enclosed in [13]. The channel mismatches were recalculated by using the calibration signal, when channel parameters change dynamically in TIADCs [14].

An autocorrelation function of each ADC's output was used to determine the timing skew mismatch between adjacent channels in TIADCs [15]. The analog transfer function of each channel was modeled including the sampling time and correction filters were designed for cancellation of distortions [16]. A technique which uses statistics of the input signal to continuously estimate and eliminate the conversion errors resulting from offset, gain, and timing mismatch was proposed [17].

A fully digital background algorithm was used to estimate and correct the timing mismatch errors between four interleaved channels [18]. The timing skew mismatches estimation methods for operating in the background, i.e., without interrupting the normal conversion, was reported [19]. A systematic overview of various calibration methods for timing skew in time interleaved analog-to-digital converters (TIADCs) was provided [20]. Architectures of 4-channel mixing-filtering-processing (MFP) digitizers were presented and evaluated [21].

Even though distinct techniques were followed in different optimization algorithms, almost all of them have a common configuration, given in Fig.3. The different operations carried out in the algorithms are described below.

Population initialization is the process of assigning a prescribed number (population) of random solutions to whatever parameter which is to be optimized. The initialized values are represented as a vector X_{ik}. Here the index *i* represents the i^{th} parameter and the *'k'* represents the k^{th} value in a population of *'p'*. Genetic operators like crossover, mutation etc are used to generate new solutions during reproduction process. The resulting vector after these operations is represented as X'_{ik}. The quality of the candidate solutions in the current population is determined by calculating the fitness values.

The fitness values are calculated using fitness function, which is a function of error signal. In the present case error signal *e(n)* is the difference between the output signal $x_p(n)$ from TIADCs without mismatches and the corrected signal $x_c(n)$ from TIADCs with mismatches. Based on the values of fitness function, the selection operator selects the candidate solutions which are to be retained in the next generation. The reproduction, fitness evaluation and selection operations run continuously in a loop, known as iterations, until the fitness of the solution is satisfactory and this solution gives the estimated values of the mismatch parameters.

Major optimization algorithms engage similar operations explained above and they only differ in operations carried out during reproduction process. The optimization algorithms which were suggested for compensation of mismatches in TIADCs and results obtained are enclosed in the following sections.

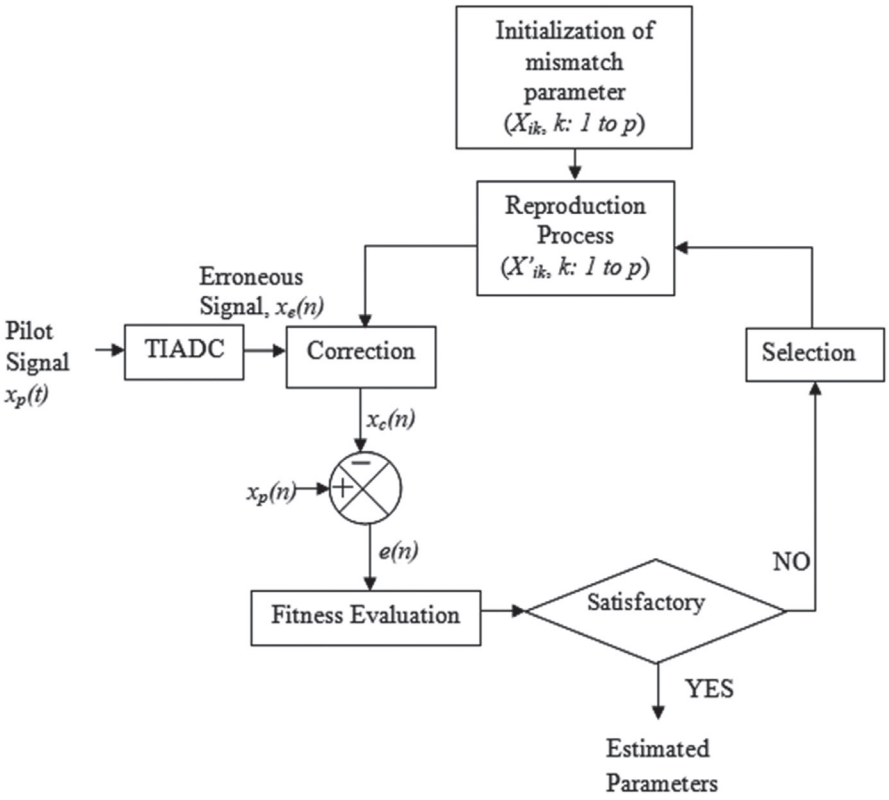


Fig. 3. Generalized block diagram for estimation of mismatches using optimization algorithms

2.1. DIFFERENTIAL EVOLUTION ALGORITHM

2.1.1. Algorithm

The differential evolution (DE) algorithm successfully estimates the mismatches with least number of iterations. As mentioned in the previous section that the algorithms differ in their operations carried out during reproduction process, DE algorithm executes two operations called as mutation and recombination, during reproduction process. During mutation operation, the difference of two random vectors with a weight of F is added to the third vector X_{ik}. The weight F of the difference is called as mutation factor. The resulting vector Y_{ik} is called as donor vector and is given by (1).

$$Y_{ik} = X_{ik} + F[X_{ik}(rand1) - X_{ik}(rand2)] \quad (1)$$

During recombination the trial vector X'_{ik} is obtained by recombining the elements of the target vector X_{ik}, and donor vector Y_{ik} as given in (2). Elements of the donor vector Y_{ik} are moved to trial vectorX'_{ik} with probability called as cross-over ratio (CR).

$$X'_{ik} = \begin{cases} Y_{ik} & if \quad rand(p) \leq CR \\ X_{ik} & if \quad rand(p) > CR \end{cases} \quad (2)$$

The selection operation is analogous to any other algorithm as explained in the previous section.

2.1.2. Estimation and correction of mismatches

The sampling time mismatches were estimated for 4-channel TIADCs using the proposed DE algorithm and was implemented in MATLAB [5]. The erroneous signal in each channel was corrected by delaying the signal with a delay equal to estimated sampling time mismatch. For delaying the signal, a fractional delay filter of 6 coefficients was used.

The suggested algorithm was assessed with various input signals like speech, sinusoidal and AM. The evaluation was carried out by calculating signal quality measuring parameters like SNR and SNDR. Table 1 shows the functional parameter values used the current work.

Table 1. DE algorithm parameters

S. No.	Parameter	Value
1.	Mutation Factor (F)	0.8
2.	Cross Over Ratio (CR)	0.4
3.	Population (p)	20
4.	Channels (N)	4

The initial population p of the parameter X_{ik} was taken as 20. A 6-tap fractional delay filter was used for correction of errors due to sampling time mismatches. The correction was implemented with TIADC input signals such as sinusoidal, speech, and amplitude modulated (AM) signals.

During the estimation of sampling time mismatches using DE, the convergence of the sampling time mismatches ($\Delta t_i'$) for a 4-channel TIADCs is shown in Fig. 4, where the actual mismatches introduced were (0.00, 0.02, 0.01, 0.015). The number of iterations (it_{max}) was the termination criterion which in this case was equal to 10.

The termination criterion can be either a predefined number of iterations or fitness function value. If the termination criterion is minimization of fitness function value, then the variation of number of iterations required for various fitness function values is shown Fig. 5.

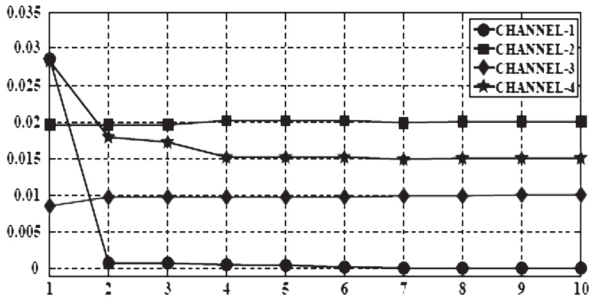


Fig. 4. Convergence of sampling time offsets during estimation by DE

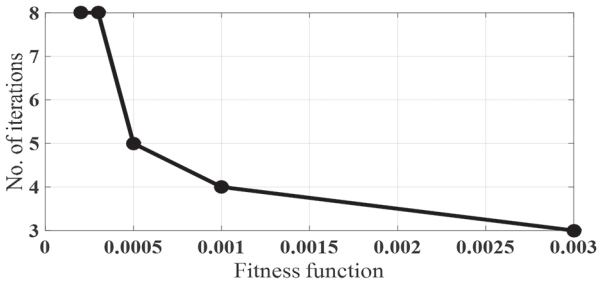


Fig. 5. Change in no. of iterations w.r.t fitness function

2.1.3. Estimation and correction in an OFDM receiver

The sampling time mismatch, gain mismatch and dc offsets were estimated for 7-channel TIADCs using the proposed DE algorithm. The algorithm was implemented in MATLAB. The DE algorithm specific parameters are listed in the following Table 2.

Table 2. DE algorithm parameters used for OFDM

Parameter	Range	Value Used
Mutation Factor, F	[0-2]	0.7
Cross Over Ratio, CR	[0-1]	0.5
Initial population, p	-	20

The termination criterion in this case is the number of iterations. The proposed algorithm used 50 iterations for estimation of mismatches. The number of iterations increases if the values of the mismatches to be estimated are very small.

The estimation was accurate and the estimated mismatches were very close to the introduced mismatches in the TIADCs. The convergence of the estimated dc offsets ($\Delta I_i'$), gain mismatches ($\Delta g_i'$) and sampling time mismatches ($\Delta t_i'$) towards their actual values (introduced) in 7- channel TIADCs are shown in Figures 6(a),(b)&(c) respectively. The mismatches in TIADCs were corrected in OFDM channel having awgn noise in the range 4-20dB. The SNDR for 7-channel TIADCs was improved by 42dB and 54dB for 6-bit and 8-bit precisions respectively for a sinusoidal input signal with a normalized frequency of 0.45.

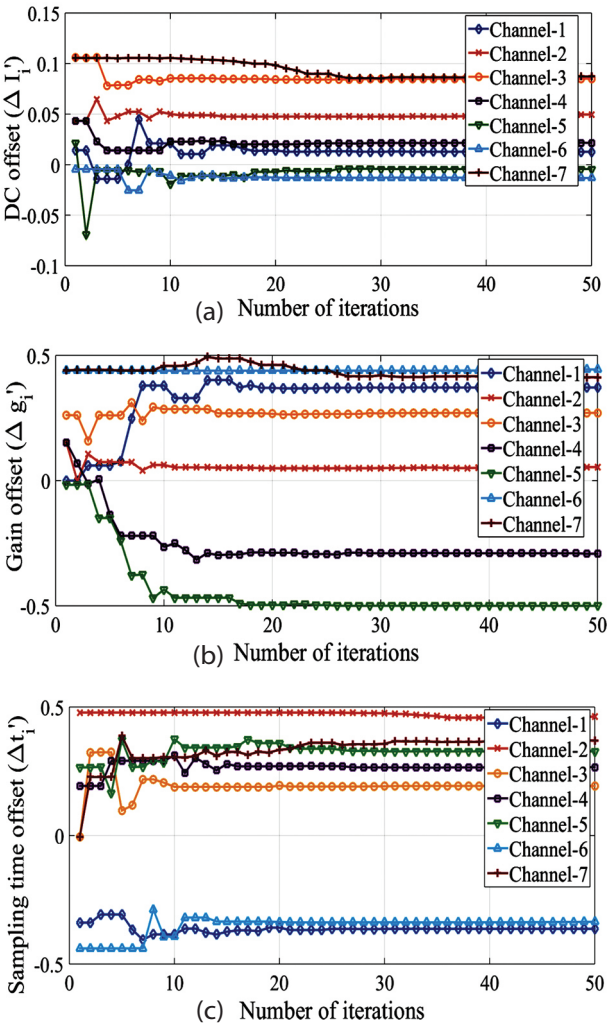


Fig. 6 (a),(b),(c). Convergence of dc, gain and sampling time offsets

2.1.4. DE algorithm implemented on FPGA

The DE algorithm implemented here was modified slightly and the differences are given below.

- Order in which the selection and reproduction operations were carried out.
- During reproduction only mutation was performed. There was no recombination operation.

A Field programmable gate array (FPGA) board was used for implementing the algorithm and correction was applied in MATLAB. The power utilization of FPGA kit and IO ports used for TIADCs with 4 and 2 channels are tabulated in Table 3.

Accurate estimation of sampling time mismatches was achieved using the algorithm. The algorithm employs a sinusoidal signal as a pilot signal. The correction was carried out by applying sinusoidal as well as speech input signals to TIADCs. SNR, SNDR, SFDR and PSNR were determined for evaluating the performance of the algorithm. A significant improvement was noticed in the parameters mentioned above. VHDL programming was used for implementing the algorithm for TIADCs with 2 and 4 channels. The algorithm was checked on NEXSYS-4 Double Data Rate (DDR) FPGA board. Fig. 7 shows the FPGA board used.

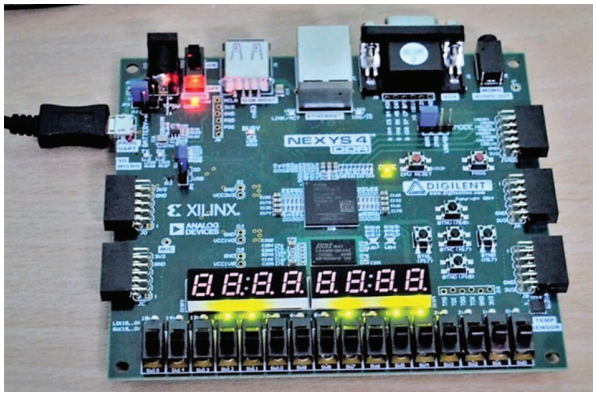


Fig. 7. NEXSYS-4 DDR FPGA board

In this technique, sinusoidal input signal was sampled and the samples were represented in 10 bit digital form. The coefficients of a 6-tap fractional delay filter, used for correction of sampling time mismatches, were generated in MATLAB. The synthesis results and summary of various parameters used during implementation are given in Table 3.

As the estimated sampling time mismatches $(\Delta t_i')$ were in 10-bit binary form, for TIADCs with 2 and 4 channels the number of output ports required was 20 and 40 respectively.

The signal at the input of each channel in TIADCs was delayed with the estimated sampling time mismatch of $\Delta t_i'$. The convergence of the sampling time mismatches $(\Delta ti')$ during their estimation for 4-channel TIADCs is shown in Fig. 8. The actual mismatches introduced were (0.01, 0.04,-0.04, 0.12).

Table 3. Implementation parameters and synthesis results

Parameter	Channels	
	N = 4	N = 2
Test Signal (Sinusoidal) Normalized Frequency (f)	0.03125	0.03125
ADC precision (No of bits)	10	10
Fractional Delay Filter Coefficients	6	6
I/O Ports used on FPGA Board	40	20
I/O Utilization	27%	13%
Total On-chip power	57mW	57mW

As the estimated sampling time mismatches $(\Delta t_i')$ were in 10-bit binary form, for TIADCs with 2 and 4 channels the number of output ports required was 20 and 40 respectively.

The signal at the input of each channel in TIADCs was delayed with the estimated sampling time mismatch of $\Delta t_i'$. The convergence of the sampling time mismatches $(\Delta t_i')$ during their estimation for 4-channel TIADCs is shown in Fig. 8. The actual mismatches introduced were (0.01, 0.04,-0.04, 0.12).

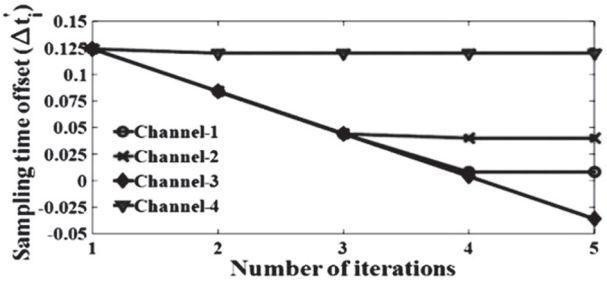


Fig. 8. Convergence of sampling time offsets

2.2. GENETIC ALGORITHM

2.2.1. Algorithm

The Genetic algorithm (GA) was also employed for estimation of sampling time mismatch and perfect reconstruction of the signal from its samples was accomplished. In GA the first step is initialization, where the mismatch parameters are initialized with a random set of values. The initialized values are known as chromosomes (Chr). The next step involves reproduction process, in which two operations called as crossover and mutation are performed. These two operations are described underneath.

Cross over: Any two initialized chromosomes (Chr) in binary form are selected randomly. After that, by choosing a cross over point (COP) the bits either before or after the cross over point are interchanged. The COP is chosen randomly and some times more than one COP are chosen. The cross over operation is illustrated in Table 4. The chromosomes (Chr) resulting from cross over are called as child chromosomes.

Table 4. Cross over operation

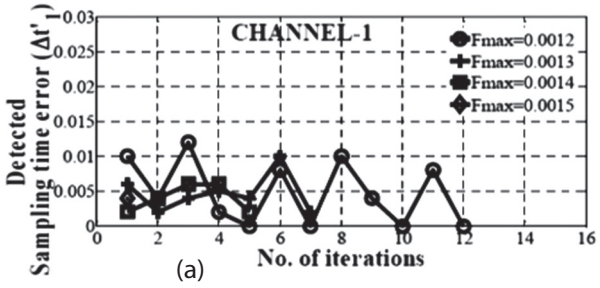
Chromosome	Binary							
25	0	0	0	1	1	0	0	1
54	0	0	1	1	0	1	1	0
						COP		

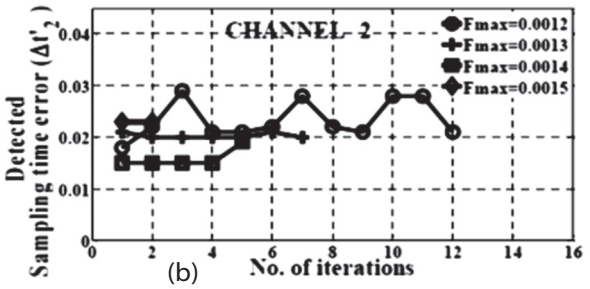
Mutation: Once the child chromosomes are obtained, one bit is chosen randomly in each child chromosome and it's mutated i.e., replace '0' with '1' and '1' with '0'.

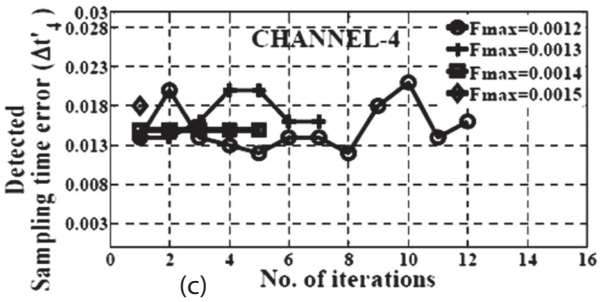
After performing these two operations the chromosome values are once again converted back to decimal values.

2.2.2. Estimation and correction using GA

GA based algorithms were used for calibration of sampling time mismatches in TIADCs with four channels [2, 6]. The pilot signal used was a single tone sinusoidal signal. The sampling time mismatches (Δt_i) in TIADCs were estimated with an accuracy of 3 decimal points. The correction was carried out with a fractional delay filter of 6 coefficients. An improvement in SNR was observed after correction. The convergence plots of estimated sampling time mismatches (Δt_i) for TIADCs four channels are shown in Fig. 9.(a),(b),(c),(d). Here the introduced mismatches are (0.000, 0.020, 0.010, 0.015) and the fitness evaluation parameter (F_{max}) are varying from 0.012 to 0.014.







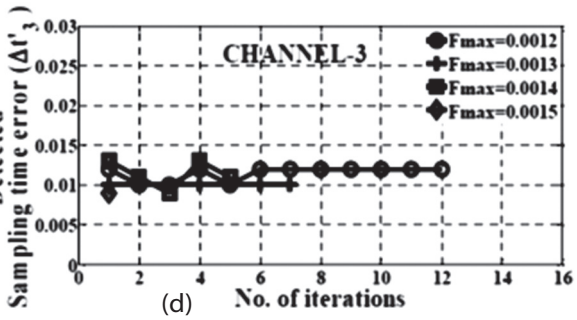


Fig.9. (a), (b), (c), (d) Convergence of sampling time offsets for 4-channel TIADCs

The number of iterations required for convergence with respect to fitness function values is shown in Fig.10.

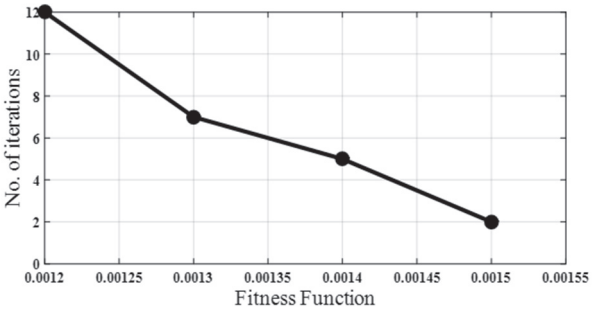


Fig.10. Variation in no. of iterations w.r.t fitness function

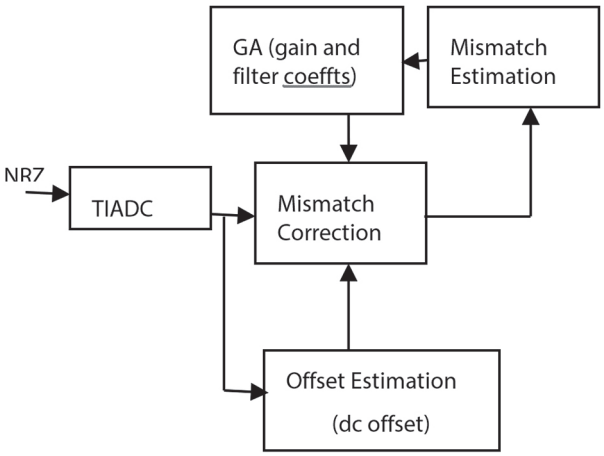


Fig.11. Estimation and correction

A foreground calibration mechanism employing GA together with a error estimation and correction method was proposed [2]. Joint estimation of static and frequency-dependent parameters was carried out by the employed detection technique comprising of GA. The proposed technique designed a notch filter to estimate the mismatches from the TIADC output. The presence of mismatches results in mismatch spurs in TIADC output. A notch filter was used to estimate the mismatches by eliminating the input frequency. Further, the power of the signal, with mismatch only, was pulled out and the total amount of mismatch was estimated. A mul-

tiple notch filter was designed with different cut-off frequencies. A foreground multitone signal, which was generated by a non-return-to-zero (NRZ) source, was applied as TIADC input. The above method corrects the offset and gain mismatches by direct multiplications and additions. Constant coefficient derivative filters were used to calibrate the frequency-dependent mismatches. The gain and filter polynomial coefficients were determined using GA and the channels' offset mismatches (dc offsets) were estimated by taking the mean of the output from each channel. The block diagram of this method is shown in Fig. 11.

3. PERFORMANCE COMPARISON OF THE ALGORITHMS

The optimization algorithms used for estimation and subsequent correction of mismatches in TIADCs are compared with respect to quality of the reconstructed signal. Signal quality metrics like signal to noise ratio (SNR), signal to noise and the distortion ratio (SNDR) and also number of iterations were used for comparison. Sinusoidal signal (Single tone) was applied as input signal to 4-Channel TIADCs and the reconstructed signal's quality was evaluated. Table 5 show cases the performance comparison of different algorithms.

Table 5. Performance comparison algorithms

	Algorithm				
		DE		GA	
Reference .No	[3]	[1]	[5]	[6]	[2]
No. of Channels (N)	4	7	4	4	4
Mismatch type	Timing	Dc , gain and timing	Timing	Timing	Timing, dc, gain and bandwidth
Filter Length	6	-	6	6	12
Normalized Frequency (f) range	0-0.45	0-0.45	0-0.45	0-0.4	0-0.5
Max.SNR (dB) (For single tone input)	67	-	63	71	65
Max. SNDR (dB) (For single tone input)	70	54	100	-	-
No. of iterations for convergence	5	30 (For 3 parameters)	4	12	100 (For 4 parameters)

4. CONCLUSION AND FUTURE SCOPE

Optimization algorithms applied in signal processing provides a scope for interdisciplinary research and application of those algorithms in solving diverse engineering problems. Optimization algorithms like DE and GA were used effectively for estimation of mismatches in TIADCs. Upon observation of the convergence plots, DE algorithm required less number of iterations and hence it is fast converging for the current problem sphere. However, as the algorithms were tested by simulation, the efficacy of these algorithms can be judged with more reliability by implementing them in hardware. The correction applied using the estimated mismatches provided a noteworthy improvement in signal quality in terms of SNR and SNDR. Moreover, since a wide range of optimization algorithms are available, the effectiveness of other algorithms, apart from the algorithms covered in the current review, can be tested.

5. REFERENCES

[1] M. V. N. Chakravarthi, B. Chandramohan, "Calibration of offsets in Time Interleaved ADCs in an OFDM receiver using differential evolution algorithm", Optoelectronics, Instrumentation and Data Processing, Vol. 57, No. 3, 2021, pp. 287-296.

[2] Y. A. Tavares, M. Lee, "A Foreground Calibration for M-Channel Time-Interleaved Analog-to-Digital Converters Based on Genetic Algorithm", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 68, No. 4, 2021, pp. 1444-1457.

[3] M. V. N. Chakravarthi, B. Chandramohan, "Estimation and correction of sampling time offsets in TI-ADCs using optimization algorithm", International Journal of Innovative Technology and Exploring Engineering, Vol. 9, No. 4, 2020, pp. 1217-1222.

[4] Q. Yongtao, J. Zhou, Y. Liu, Y. Huangfu, "A Novel Calibration Method of Gain and Time-skew Mismatches for Time-interleaved ADCs Based on Neural Network", Proceedings of the IEEE MTT-S International Wireless Symposium, Guangzhou, China, 19-22 May 2019, pp. 1-3.

[5] M. V. N. Chakravarthi, B. Chandramohan. "Estimation of sampling time offsets in an N-channel time-interleaved ADC network using differential evolution algorithm and correction using fractional delay filters", Machine Intelligence and Signal Analysis, pp. 267-278. Springer, Singapore, 2019.

[6] M. V. N. Chakravarthi, B. Chandramohan, "Detection and Correction of Sampling-Time-Errors in an N-Channel Time-Interleaved ADC using Genetic Algorithm", Proceedings of the 14th IEEE India Council International Conference, Roorkee, India, 15-17 December 2017, pp. 1-6.

[7] W. Jun-Shan, S.-J. Liu, P.-P. Qi, "An optimization algorithm for timing-error estimation in time-interleaved ADCs", Proceedings of the IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, Xi'an, China, 29 October - 1 November 2012, pp. 1-3.

[8] C. Shuai, L. Wang, H. Zhang, Rosanah Murugesu, Dustin Dunwell, Anthony Chan Carusone, "All-digital calibration of timing mismatch error in time-interleaved analog-to-digital converters", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 25, No. 9, 2017, pp. 2552-2560.

[9] G. Jian, P. Ye, H. Zeng, Jinpeng Song, Wentao Wei, Kuojun Yang, "An adaptive calibration technique of timing skew mismatch in time-interleaved analog-to-digital converters", Review of Scientific Instruments, Vol. 90, No. 2, 2019, p. 025102.

[10] T. Van-Thanh, V.-P. Hoang, V.-P. Pham, C.-K. Pham, "An Improved All-Digital Background Calibration Technique for Channel Mismatches in High Speed Time-Interleaved Analog-to-Digital Converters", Electronics, Vol. 9, No. 1, 2020, p. 73.

[11] B. Xu, H. Hu, W. Li, F. Liu, "Blind calibration method for two-channel time-interleaved analog-to-digital converters based on FFT", Journal of Electronic Testing, Vol. 34, No. 6, 2018, pp. 643-650.

[12] L. Jian, J. Li, S. Wu, N. Ning, Y. Liu, "A Bandwidth Mismatch Optimization Technique in Time-Interleaved Analog-to-Digital Converters", Journal of Circuits, Systems and Computers, Vol. 28, No. 6, 2019, p. 1950090.

[13] C. D. Kenneth, J. P. Keane, S. Lewis. "Calibration and dynamic matching in data converters: Part 2: Time-interleaved analog-to-digital converters and background-calibration challenges", IEEE Solid-State Circuits Magazine, Vol. 10, No. 3, 2018, pp. 61-70.

[14] L. Sujuan, N. Lv, H. Ma, A. Zhu, "Adaptive semiblind background calibration of timing mismatches in a two-channel time-interleaved analog-to-digital converter", Analog Integrated Circuits and Signal Processing, Vol. 90, No. 1, 2017, pp. 1-7.

[15] L. Xin, J. Wu, C. Vogel, "A Background Correlation-Based Timing Skew Estimation Method for Time-Interleaved ADCs", IEEE Access, Vol. 9, 2021, pp. 45730-45739.

[16] M. Pietro, F. Rosato, A. Trifiletti, "New models for the calibration of four-channel time-interleaved ADCs using filter banks", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 65, No. 2, 2017, pp. 141-145.

[17] M. Hamidreza, M. Yargholi, M. Yavari, "Digital blind background calibration of imperfections in time-interleaved ADCs", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 64, No. 6, 2017, pp. 1504-1514.

[18] A. Abbaszadeh, E. N. Aghdam, Alfredo Rosado-Muñoz, "Digital background calibration algorithm and its FPGA implementation for timing mismatch correction of time-interleaved ADC", Analog Integrated Circuits and Signal Processing, Vol. 99, No. 2, 2019, pp. 299-310.

[19] A. Sarkis, M. Ehsanian, "Generalized Method for Extraction of Offset, Gain, and Timing Skew Errors in Time-Interleaved ADCs", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 67, No. 7, 2019, pp. 1214-1218.

[20] L. Xin, C. Huang, D. Ding, J. Wu, "A review on calibration methods of timing-skew in time-interleaved ADCs", Journal of Circuits, Systems and Computers, Vol. 29, No. 2, 2020, p. 2030002.

[21] L. Sujuan, H. Ma, N. Lyu, H. Wang, "Adaptive blind timing mismatch calibration with low power consumption in M-channel time-interleaved ADC", Circuits, Systems, and Signal Processing, Vol. 37, No. 11, 2018, pp. 4861-4879.