Seven-Level Symmetrical Series/Parallel Multilevel Inverter with PWM Technique Using Digital Logic

Original Scientific Paper

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Abstract *– This paper attempts to come up with a proposed configuration of Multilevel inverters with a lesser number of switches that are smaller in size, lesser in cost and with a higher efficiency. Designing an inverter topology with a lesser number of switches and proper control technique is the major challenge. cascaded H-Bridge (CHB) topology are more popular among the existing configurations of multilevel inverters (MLI). Even though it can produce more levels, it needs to accommodate a huge number of switches for higher levels. The focus of this paper is to reduce the number of components for the same voltage level of cascaded H-Bridge configuration. In addition to that, generating the gating pulses for the switches is difficult when there is an asymmetry in the switches. A new symmetrical series/parallel configuration is proposed with reduced switch count and the pulse width modulation (PWM) technique is implemented with digital logic to generate the required gating pulses for the switches. The total harmonic distortion (THDI) of the output current is reduced with this PWM technique. The simulation has been carried out in MATLAB/Simulink software for both R (resistive) and R-L (resistive -inductive) loads.*

Keywords *– Renewable energy sources (RES); Multilevel inverter (MLI); pulse width modulation (PWM) technique; Total harmonic distortion (THD); Cascaded H-bridge (CHB) inverter*

1. INTRODUCTION

There is a rapid increase in the penetration of power electronic converters in the industry. Amongst many power electronic converters a multilevel inverter plays a vital role in the conversion of DC to AC. The multilevel inverter is known for its efficient functioning, especially in high power applications. The world is swiftly moving towards the usage of electric vehicle technology as the best alternative for the internal combustion engines. These electric vehicles are run by an induction motor, which is fed by multilevel inverters. Apart from this, the fossil fuels which supply the major part of electrical energy in the world are diminishing continuously, and the world is relying on renewable energy sources (RES) [1-7] like the photovoltaic (PV) system [8-13], wind energy and fuel cell energy systems. In [1], the authors have used the inverter controller for renewable energy sources and to examine the role, importance, and functioning of the inverter. The inverter was being used for the electric vehicle application with an objective to propose a new controller. [2]. A new control scheme had also been explained to integrate renewable energy sources into the distribution system [7]. In [12], the authors have also developed a bidirectional inverter for PV based power generation system. However, the authors [1-7, 12] did not consider the multilevel inverters in their research. The nature of supply and magnitude of voltage from these renewable energy sources do not match with load or grid requirements. Hence, there arises a need to use a power electronic converter for power conversion. Conversion from DC to AC is done by an inverter. Fig. 1 shows the simple block diagram of the grid-connected single-stage photovoltaic system using a multilevel inverter. Converting to AC supply with a fewer harmonic (THD) [14-18] is the requirement and it is a major challenge to achieve the same. However, the authors proposed controllers to reduce THD in [15, 16] by using a multilevel inverter, but due to the

high number of switches, the THD is more as compared to the proposed structure in this paper. The existing two-level inverter can produce the alternative supply, but it consists of more harmonics as the wave shape is a square wave.

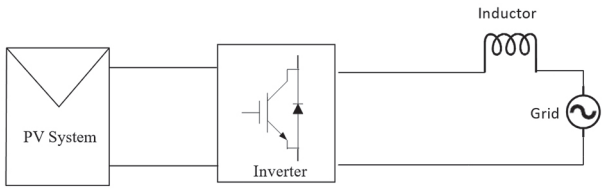


Fig. 1. The photovoltaic system connected to the grid

Multilevel inverters (MLI) [19-27] are introduced to improve the wave shape near to sinusoidal and also to minimize the harmonics in the power supply. There are different types of multilevel inverters like diode-clamped, flying-capacitor, and cascaded H-Bridge type inverters. But, the cascaded H- Bridge type inverter works successfully. The major setback of this Cascaded H-Bridge (CHB) is, the required number of components is more for high voltage levels. Therefore, the cost and size of the inverter increases along with switching losses. Recently, many researchers proposed different structures for multilevel inverters along with suitable control strategies [19-27]. Among many structures, some topologies were developed with a fewer number of switches. The multilevel inverters with a fewer number of switches are widely used in many applications including electric vehicles and renewable energy source-based electrical power generation systems for AC applications [28-31].

Although there are higher-level inverter configurations, seven-level inverters became popular for many industrial applications like direct torque control of induction motor and in traction systems. Also, for a higher-level topology, the cost of an inverter will increase. Hence for considering the economical factor, seven-level inverter is considered in this paper. This paper presents a new topology with a fewer number of switches and components. The focus of this paper is onreducing the number of switches and control pulses forthose switches, using the pulse width modulation (PWM) technique. A seven-level symmetrical series/parallel topology is proposed in this paper with a fewer number of components. Also, the controllingof switches through gating pulses using a pulse width modulation technique is a challenge when there is an asymmetry in the configuration concerning switches. In general, 3 carriers would be required for a seven-level voltage, and we get three gating signals. In the case of the Cascaded H-Bridge CHB inverter, three signals are given to three H Bridges top switches and bottom switches are given by the same signals using NOT gate. But, in the case of this proposed topology, there were eight switches and was difficult to give the gating pulses. Hence, a digital pulse width modulation (DPWM) technique is implemented for this configuration. The circuit was simulated in MATLAB/Simulink platform and the results were presented and evaluated for both R and RL loads. The THDI and THDV are also measured.

2. seven-level SYMMETRICAL SERIES/ PARALLELCONFIGURATION

The proposed configuration of the seven-level symmetrical series-parallel multilevel inverter for RL- load is shown in Fig. 2. Three voltage sources of $V_{DC}/3$ were taken and those are connected to load in different combinations of series and parallel to get various output voltage levels. One H-Bridge is used at the load end with four switches and another four switches are connected at the source side. A total of eight switches are required.

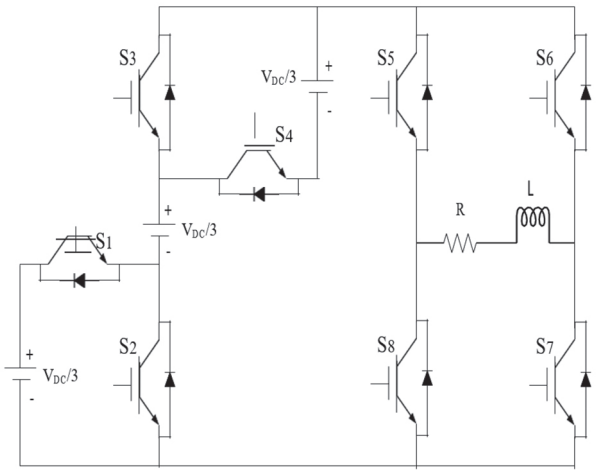


Fig. 2. Configuration of seven-level symmetricalseries/parallel inverter

Table 1 shows the switching sequence for the seven-level symmetrical series/parallel inverter configuration. The voltage levels of V_{DC}, $2V_{DC}/3$, $V_{DC}/3$, 0, $-V_{DC}/3$, $-2V_{DC}/3$, and $-V_{DC}$ voltage levels can be obtained by operating the switches by giving gating pulses. Which switch is operating for the corresponding voltage level is given in Table 1.

Table 1. Switching sequence

Voltage level	Sequence of switching							
	S1	S2	S3	S4	S5	S6	S7	S8
V_{DC}	1	0	0	1	1	0	1	0
$2V_{DC}/3$	0	1	0	1	1	0	1	0
$V_{DC}/3$	0	1	1	0	1	0	1	0
0	0	0	0	0	1	1	0	0
$-V_{DC}/3$	0	1	1	0	0	1	0	1
$-2V_{DC}/3$	0	1	0	1	0	1	0	1
$-V_{DC}$	1	0	0	1	0	1	0	1

The current path and switches operating for each voltage level is explained with diagrams below.

Fig. 3 shows the diagram for the zero voltage level. In this case, switches S_5 and S_6 are ON which causes to short the load and zero volts appear across the load.

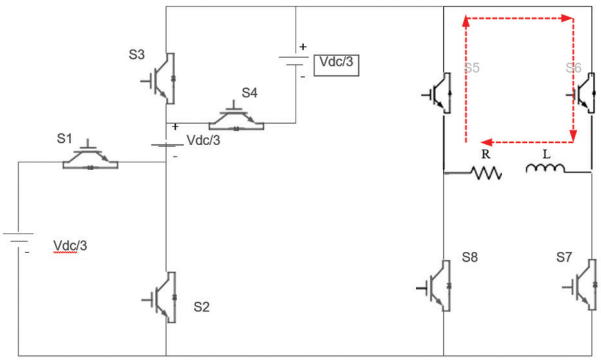


Fig. 3. Switching state 1

Fig. 4 shows the diagram for the VDC/3 voltage level. In this case switches S_2, S_3, S_5, and S_7 are ON and the voltage across the load is VDC/3 volts.

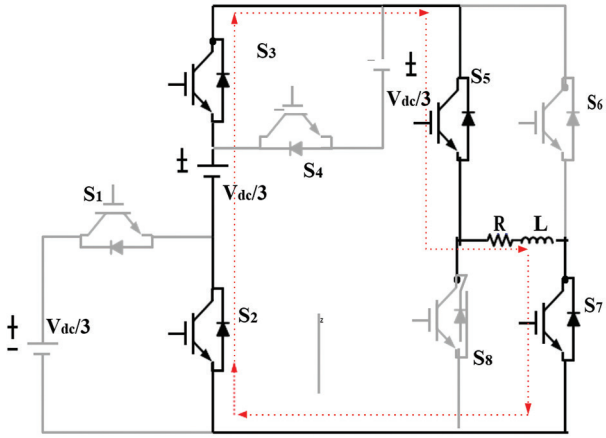


Fig. 4. Switching state 2

Fig. 5 shows the diagram for the $2V_{DC}/3$ voltage level. In this case switches S2, S4, S5, and S7 are ON and the voltage across the load is $2V_{DC}/3$ volts.

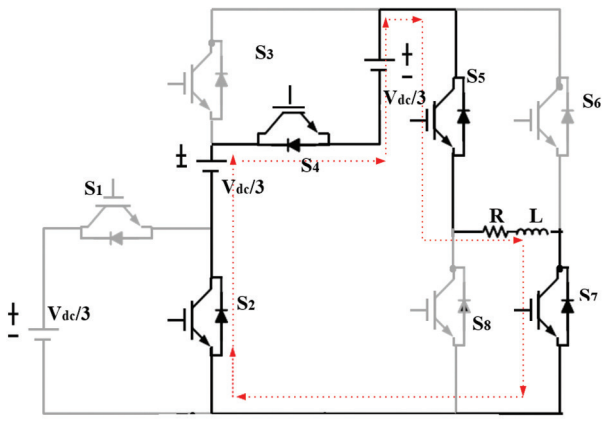


Fig. 5. Switching state 3

Fig. 6 shows the diagram for the V_{DC} voltage level. In this case switches S_1, S_4, S_5, and S_7 are ON and the voltage across the load is V_{DC} volts.

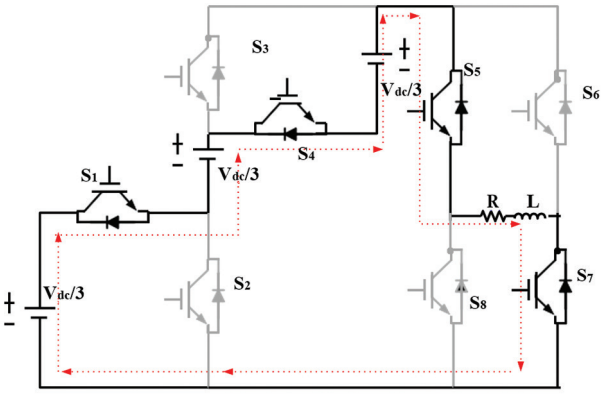


Fig. 6. Switching state 4

The comparison between capacitor clamped, diode clamped, and Cascaded H-Bridge multilevel inverter configurations with the proposed 7-level inverter are listed in Table 2.

Table 2. Comparison of different configurations

Parameter	Capacitor clamped inverter [22]	Diode clamped inverter [22]	Cascaded H-Bridge (CHB) inverter	Proposed inverter [22]
Diodes	0	12	0	0
Capacitors	10	0	0	0
Switches	12	12	12	8
sources	6	6	3	3
Anti-parallel diodes	12	12	12	8

3. PWM TECHNIQUE

The pulse width modulation control technique has been implemented to give the gating pulse to switches. As this configuration has asymmetrical switches, a simplified PWM technique is implemented with three carriers and with one reference signal. Initially, three signals A, B, C are generated using carriers and reference signals. Signal D is taken randomly high for a positive cycle and low for a negative cycle. By using these four signals switching pulses are generated with the help of logic gates. Fig. 8 shows the switching logic and signals.

The logical notation is given in below Table-3 for getting switching pulses for each switch

Table 3. Logic gating notation

S. No	Switc h	Switching Stage
1	S1	C
2	S2	$A\overline{C}$
3	S3	$A\overline{B}$
4	S4	B
5	S5	$D + \overline{AD}$
6	S6	$\overline{D} + \overline{AD}$
7	S7	AD
8	S8	$A\overline{D}$

Schematic model of switching logic is shown in Fig. 7. Three carrier wave forms of 3500 Hz frequency are compared with a sinusoidal wave form of 50 Hz frequency to generate the pulses A, B, C and D. The pulses for switches S_1 to S_8 are generated by using logic gates.

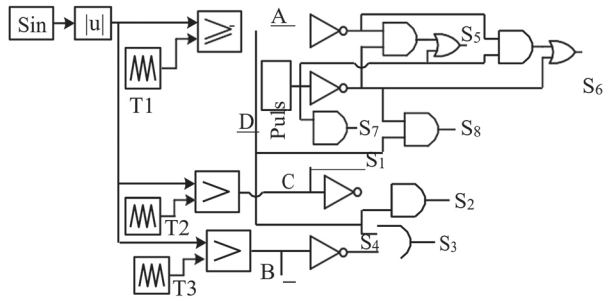


Fig. 7. Schematic model of switching logic

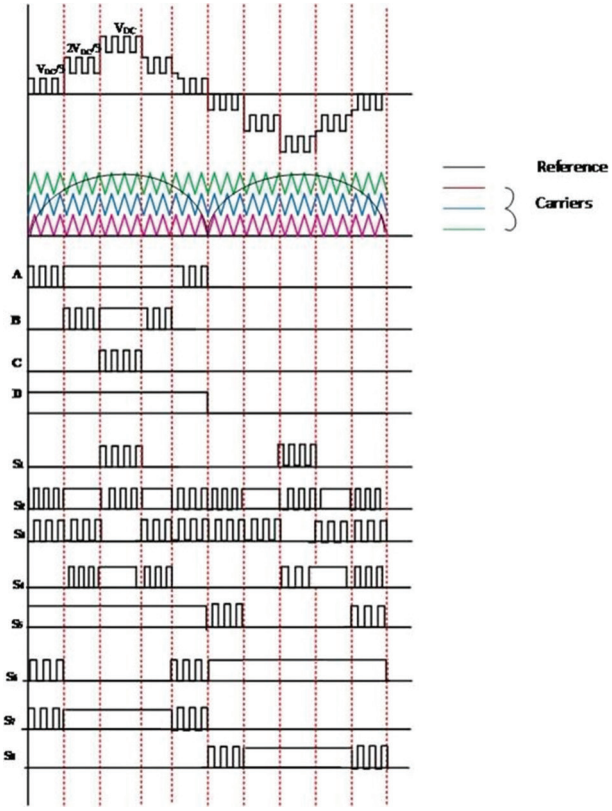


Fig. 8. PWM Technique

4. SIMULATION RESULTS

The proposed 7-level inverter was configured in MATLAB platform and implemented in Simulink. While developing a seven-level inverter, Power supply was considered as DC sources. Generally, this DC sources do not allow the currents in reverse direction or for charging. Hence, charging currents for DC sources will be required in R-L load. In the discharging mode of L. For gating pulses, Fig. 9 shows the pulses of A, B, C, and D generated by level-shifted pulse width modulation. The sinusoidal wave form is taken as a reference signal and three triangular waveforms are taken as carrier signals. By comparing this reference signal and carrier signal, pulses A, B, C are generated. Pulse D is ON for a positive half cycle and OFF for the negative half cycle.

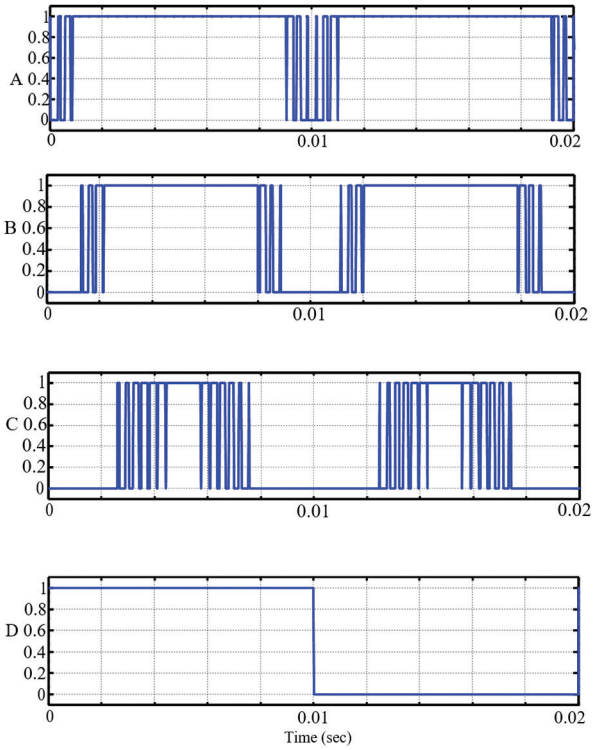
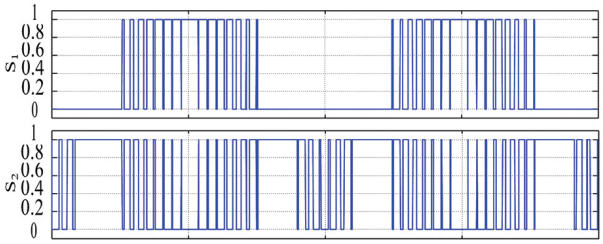


Fig. 9. PWM Pulses A, B, C and D

Fig. 10 shows the gating pulses for switches S_1 through S_8. The signals A, B, C and D are logically combined using logic gates to generate the gating pulses S_1 to S_8 as shown in Fig. 10. The same logic is implemented in MATLAB and the resulting gating pulses as shown in Fig. 12 which are same as in Fig. 10.



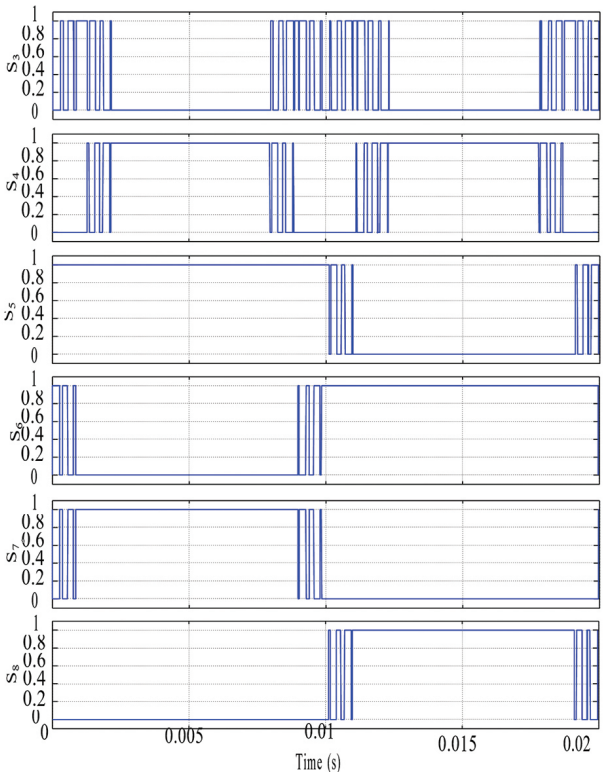


Fig. 10. Switching Pulses

Table-4 shows the Simulink circuit Parameter values.

Table 4. Simulink circuit Parameters

Parameter	Value
VDC	300 V
Load Resistance	100-ohm
Load Inductance	10 mH
Switching frequency	3500 Hz
System frequency	50 Hz
Peak Voltage	298.9 V
RMS Voltage	211.35 V
Peak Current	3.009 amp
RMS Current	2.12 amp
Filter Inductance	20 mH
Filter Capacitance	340 µF

4.1. CASE 1: R LOAD

LC filter was not considered or incorporated into the proposed inverter between load and inverter output because of testing the current THD and performance without using any filter. Hence, the current waveform will be in a similar shape as the voltage waveform with a difference in magnitude. Fig. 11 shows the seven- level PWM output voltage waveform for R-load. The magnitude of the output voltage is 300 volts and 10- ohm resistance is considered as a load. The voltage waveform and current waveforms are depicted in Fig. 11 (a) and (b) respectively. The magnitude of current will be nearly 3 amp as per system ratings.

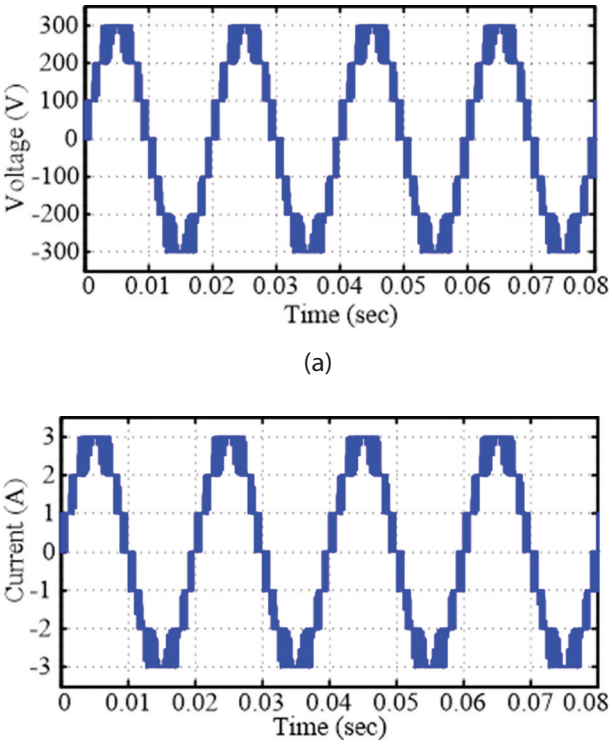
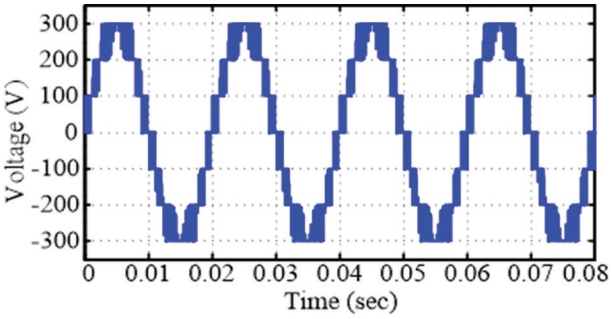
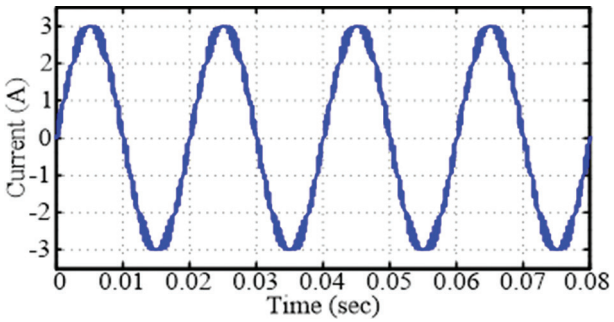


Fig. 11. Output waveforms for R load (a) Inverter output voltage (b) Load current

4.2. CASE 2: R-L LOAD

The same inverter configuration was tested for R-L load. As mentioned earlier no filter is used in this case also. However, due to load inductance, the current waveform is nearly sinusoidal. Moreover, there is no discharging path, hence there will not be any phase angle difference between voltage and current. To achieve the same magnitude of current in R load, the possible R-L is selected for comparison in THD. The voltage and current waveform for R-L load is depicted in Fig. 12 (a) and (b). Due to the absence of a filter, there will not be any significant changes in Voltage as compared to R-load. But the shape of the current is nearly sinusoidal.



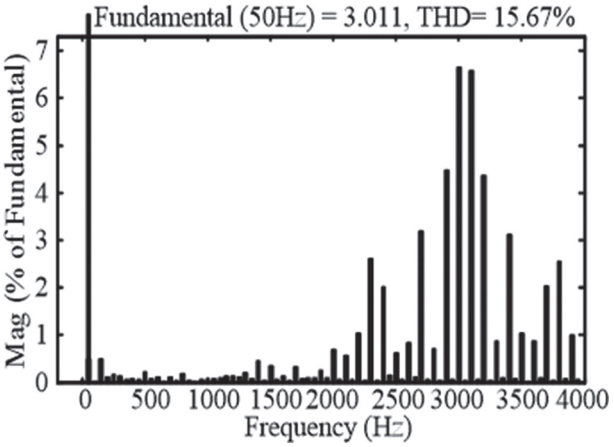


(b)

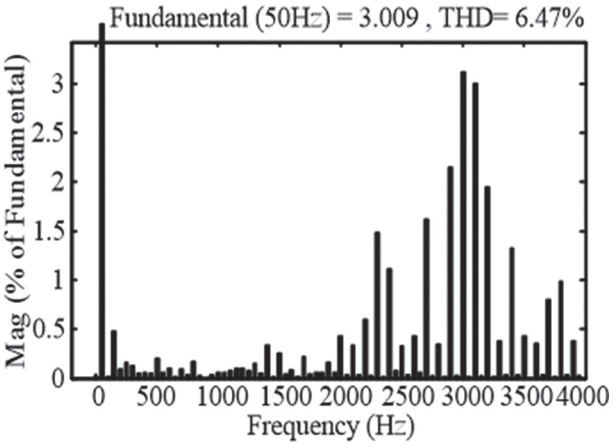
Fig. 12. Output waveforms for R-L load (a) Inverter output voltage (b) Load current

4.3. THD OF CURRENTS IN R AND R-L LOAD

The designing multilevel inverter aims to reduce THD in currents. To test the value of THD, the proposed system is designed without using any filters. For better understanding, the THDI for R load and R-L load with the same magnitude are presented in Fig. 13 (a) and (b) respectively.



(a)



(b)

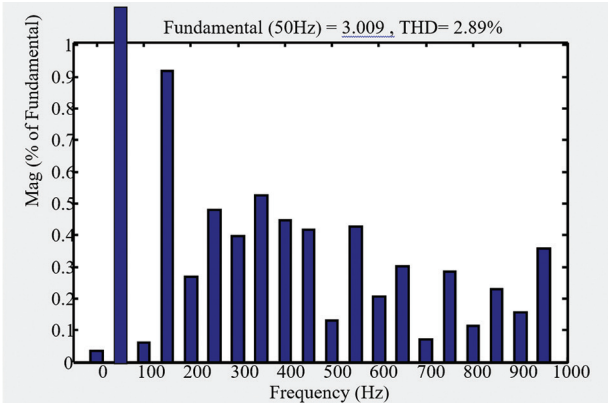
Fig. 13. FFT analysis of the current with belonging THD for (a) R load (b) R-L Load

From Fig. 13, it is clear that THD has been reduced for R-L load when compared to R-load, due to the inductance of load which acts as a filter. The lower- order harmonics are minimized, but higher-order harmonics are present. These higher-order harmonics can be minimized easily using passive filters. This will be the most benevolent feature for this proposed inverter. In general, the lower order harmonics are dangerous to the load or grid, the proposed inverter can reduce the effect of lower order harmonics and only significant magnitudes are presented in higher- order harmonics from the FFT spectrum. Further, the THDI can be minimized with a proper LC filter connected between the inverter and load.

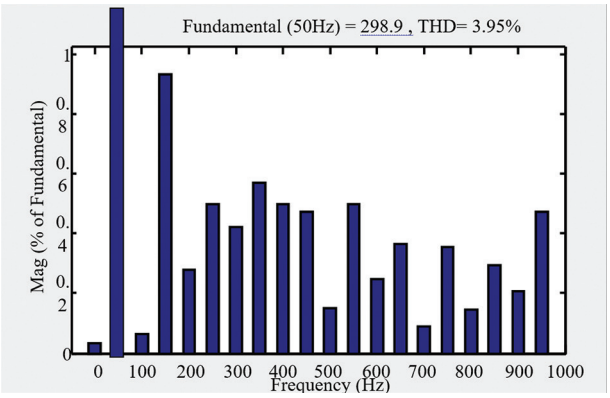
Table 5. Comparison of THDI

Parameter	Capacitor clamped inverter [22]	Diode clamped inverter [22]	Cascaded H-Bridge (CHB) inverter [22]	Proposed inverter
THDI with filter	6.8	5.7	4.9	2.9

In general, multilevel inverters are connected to load through an LC filter. Hence, the THDI and THDV for R- L load with an LC filter is shown in Fig. 14. The percentage of THDI and THDV is less than 5 percent which is allowable in the industry applications



(a)



(b)

Fig. 14. FFT analysis with belonging THD for R-L load with LC filter (a) THDI (b) THDV

5. CONCLUSION

Concludingly this is to submit that the seven-level series/parallel inverter could be implemented with a lesser number of switches and the PWM technique was applied with digital logic for this configuration. The circuit and the control logic were implemented using MATLAB software. Three voltage sources of each 100 volts were connected in series/parallel configuration using IGBT switches. The pulse width modulation technique was applied for giving the gating pulses to switches. The signals from the PWM technique were mixed by using logic gates to get the gating pulses for corresponding switches. The seven-level output voltage with the PWM technique was observed forboth R and RL loads with a magnitude of 300 volts. The current waveforms were also presented for both the loads with their THDI and THDV values. It was observed that; the effect of lower order harmonics would be reduced witha proposed inverter.

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