Volume 12, Number 3, 2021 ISSN 1847-6996

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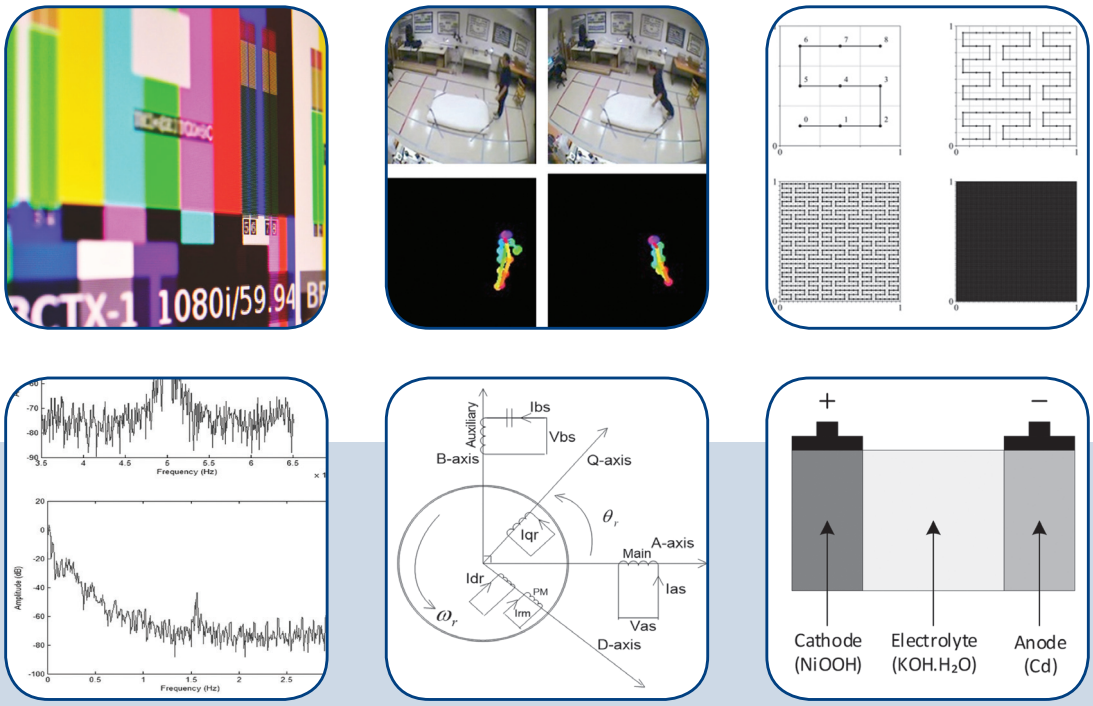
IJECES International Journal of Electrical and Computer Engineering Systems

International Journal of Electrical and Computer Engineering Systems



ISSN: 1847-6996

INTERNATIONAL JOURNAL OF ELECTRICAL AND COMPUTER ENGINEERING SYSTEMS

Published by Faculty of Electrical Engineering, Computer Science and Information Technology Osijek, Josip Juraj Strossmayer University of Osijek, Croatia

Osijek, Croatia | Volume 12, Number 3, 2021 | Pages 123-176

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International Journal of Electrical and Computer Engineering Systems (IJECES)

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Subscription Information

The annual subscription rate is 50€ for individuals, 25€ for students and 150€ for libraries.
Giro account: 2390001 - 1100016777,
Croatian Postal Bank

Journal is referred in:

- Scopus
- Web of Science Core Collection (Emerging Sources Citation Index - ESCI)
- Google Scholar
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- Genamics
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- Ulrichweb
- Reaxys
- Embase
- Engineering Village

Bibliographic Information

Commenced in 2010.
ISSN: 1847-6996
e-ISSN: 1847-7003
Published: quarterly
Circulation: 300

IJECES online

https://ijeces.ferit.hr

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Seven-Level Symmetrical Series/Parallel Multilevel Inverter with PWM Technique Using Digital Logic

Original Scientific Paper

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Abstract *– This paper attempts to come up with a proposed configuration of Multilevel inverters with a lesser number of switches that are smaller in size, lesser in cost and with a higher efficiency. Designing an inverter topology with a lesser number of switches and proper control technique is the major challenge. cascaded H-Bridge (CHB) topology are more popular among the existing configurations of multilevel inverters (MLI). Even though it can produce more levels, it needs to accommodate a huge number of switches for higher levels. The focus of this paper is to reduce the number of components for the same voltage level of cascaded H-Bridge configuration. In addition to that, generating the gating pulses for the switches is difficult when there is an asymmetry in the switches. A new symmetrical series/parallel configuration is proposed with reduced switch count and the pulse width modulation (PWM) technique is implemented with digital logic to generate the required gating pulses for the switches. The total harmonic distortion (THDI) of the output current is reduced with this PWM technique. The simulation has been carried out in MATLAB/Simulink software for both R (resistive) and R-L (resistive -inductive) loads.*

Keywords *– Renewable energy sources (RES); Multilevel inverter (MLI); pulse width modulation (PWM) technique; Total harmonic distortion (THD); Cascaded H-bridge (CHB) inverter*

1. INTRODUCTION

There is a rapid increase in the penetration of power electronic converters in the industry. Amongst many power electronic converters a multilevel inverter plays a vital role in the conversion of DC to AC. The multilevel inverter is known for its efficient functioning, especially in high power applications. The world is swiftly moving towards the usage of electric vehicle technology as the best alternative for the internal combustion engines. These electric vehicles are run by an induction motor, which is fed by multilevel inverters. Apart from this, the fossil fuels which supply the major part of electrical energy in the world are diminishing continuously, and the world is relying on renewable energy sources (RES) [1-7] like the photovoltaic (PV) system [8-13], wind energy and fuel cell energy systems. In [1], the authors have used the inverter controller for renewable energy sources and to examine the role, importance, and functioning of the inverter. The inverter was being used for the electric vehicle application with an objective to propose a new controller. [2]. A new control scheme had also been explained to integrate renewable energy sources into the distribution system [7]. In [12], the authors have also developed a bidirectional inverter for PV based power generation system. However, the authors [1-7, 12] did not consider the multilevel inverters in their research. The nature of supply and magnitude of voltage from these renewable energy sources do not match with load or grid requirements. Hence, there arises a need to use a power electronic converter for power conversion. Conversion from DC to AC is done by an inverter. Fig. 1 shows the simple block diagram of the grid-connected single-stage photovoltaic system using a multilevel inverter. Converting to AC supply with a fewer harmonic (THD) [14-18] is the requirement and it is a major challenge to achieve the same. However, the authors proposed controllers to reduce THD in [15, 16] by using a multilevel inverter, but due to the

high number of switches, the THD is more as compared to the proposed structure in this paper. The existing two-level inverter can produce the alternative supply, but it consists of more harmonics as the wave shape is a square wave.

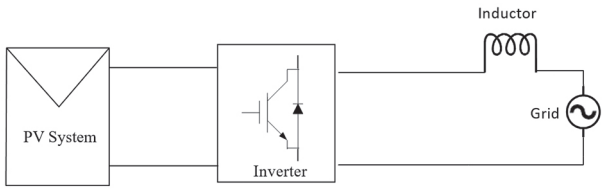


Fig. 1. The photovoltaic system connected to the grid

Multilevel inverters (MLI) [19-27] are introduced to improve the wave shape near to sinusoidal and also to minimize the harmonics in the power supply. There are different types of multilevel inverters like diode-clamped, flying-capacitor, and cascaded H-Bridge type inverters. But, the cascaded H- Bridge type inverter works successfully. The major setback of this Cascaded H-Bridge (CHB) is, the required number of components is more for high voltage levels. Therefore, the cost and size of the inverter increases along with switching losses. Recently, many researchers proposed different structures for multilevel inverters along with suitable control strategies [19-27]. Among many structures, some topologies were developed with a fewer number of switches. The multilevel inverters with a fewer number of switches are widely used in many applications including electric vehicles and renewable energy source-based electrical power generation systems for AC applications [28-31].

Although there are higher-level inverter configurations, seven-level inverters became popular for many industrial applications like direct torque control of induction motor and in traction systems. Also, for a higher-level topology, the cost of an inverter will increase. Hence for considering the economical factor, seven-level inverter is considered in this paper. This paper presents a new topology with a fewer number of switches and components. The focus of this paper is onreducing the number of switches and control pulses forthose switches, using the pulse width modulation (PWM) technique. A seven-level symmetrical series/parallel topology is proposed in this paper with a fewer number of components. Also, the controllingof switches through gating pulses using a pulse width modulation technique is a challenge when there is an asymmetry in the configuration concerning switches. In general, 3 carriers would be required for a seven-level voltage, and we get three gating signals. In the case of the Cascaded H-Bridge CHB inverter, three signals are given to three H Bridges top switches and bottom switches are given by the same signals using NOT gate. But, in the case of this proposed topology, there were eight switches and was difficult to give the gating pulses. Hence, a digital pulse width modulation (DPWM) technique is implemented for this configuration. The circuit was simulated in MATLAB/Simulink platform and the results were presented and evaluated for both R and RL loads. The THDI and THDV are also measured.

2. seven-level SYMMETRICAL SERIES/ PARALLELCONFIGURATION

The proposed configuration of the seven-level symmetrical series-parallel multilevel inverter for RL- load is shown in Fig. 2. Three voltage sources of $V_{DC}/3$ were taken and those are connected to load in different combinations of series and parallel to get various output voltage levels. One H-Bridge is used at the load end with four switches and another four switches are connected at the source side. A total of eight switches are required.

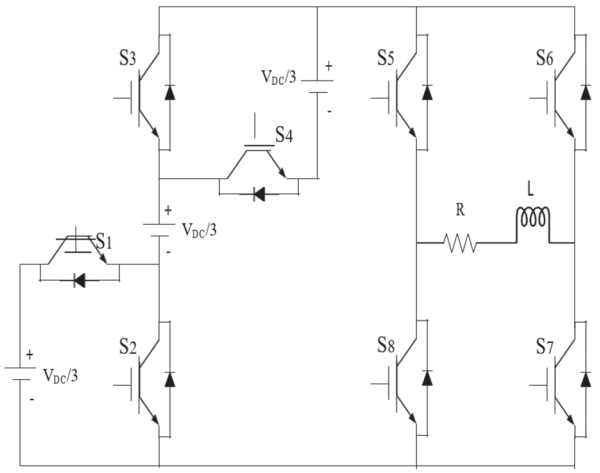


Fig. 2. Configuration of seven-level symmetricalseries/parallel inverter

Table 1 shows the switching sequence for the seven-level symmetrical series/parallel inverter configuration. The voltage levels of V_{DC}, $2V_{DC}/3$, $V_{DC}/3$, 0, $-V_{DC}/3$, $-2V_{DC}/3$, and $-V_{DC}$ voltage levels can be obtained by operating the switches by giving gating pulses. Which switch is operating for the corresponding voltage level is given in Table 1.

Table 1. Switching sequence

Voltage level	Sequence of switching							
	S1	S2	S3	S4	S5	S6	S7	S8
V_{DC}	1	0	0	1	1	0	1	0
$2V_{DC}/3$	0	1	0	1	1	0	1	0
$V_{DC}/3$	0	1	1	0	1	0	1	0
0	0	0	0	0	1	1	0	0
$-V_{DC}/3$	0	1	1	0	0	1	0	1
$-2V_{DC}/3$	0	1	0	1	0	1	0	1
$-V_{DC}$	1	0	0	1	0	1	0	1

The current path and switches operating for each voltage level is explained with diagrams below.

Fig. 3 shows the diagram for the zero voltage level. In this case, switches S_5 and S_6 are ON which causes to short the load and zero volts appear across the load.

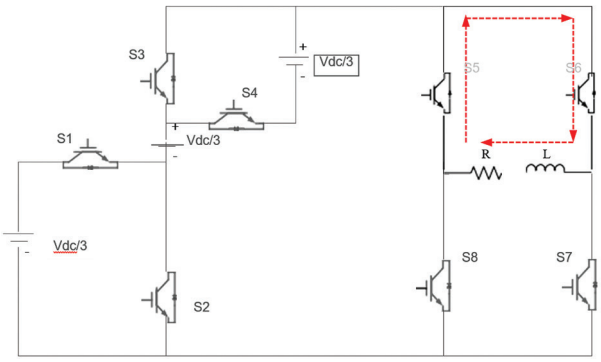


Fig. 3. Switching state 1

Fig. 4 shows the diagram for the VDC/3 voltage level. In this case switches S_2, S_3, S_5, and S_7 are ON and the voltage across the load is VDC/3 volts.

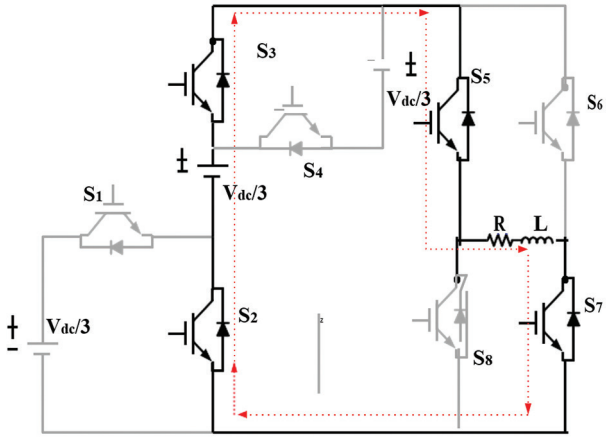


Fig. 4. Switching state 2

Fig. 5 shows the diagram for the $2V_{DC}/3$ voltage level. In this case switches S2, S4, S5, and S7 are ON and the voltage across the load is $2V_{DC}/3$ volts.

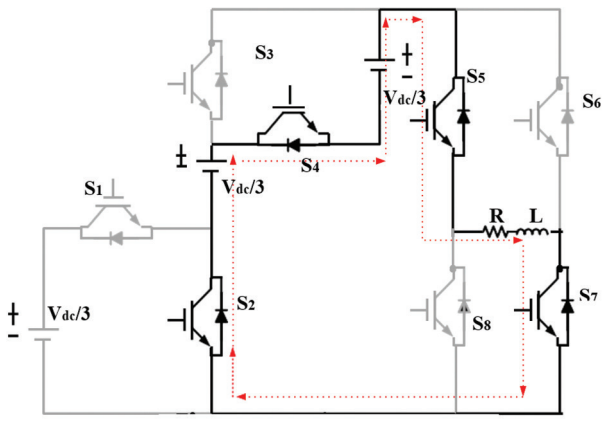


Fig. 5. Switching state 3

Fig. 6 shows the diagram for the V_{DC} voltage level. In this case switches S_1, S_4, S_5, and S_7 are ON and the voltage across the load is V_{DC} volts.

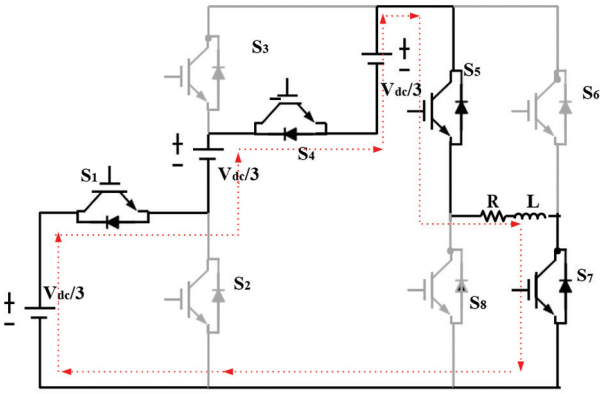


Fig. 6. Switching state 4

The comparison between capacitor clamped, diode clamped, and Cascaded H-Bridge multilevel inverter configurations with the proposed 7-level inverter are listed in Table 2.

Table 2. Comparison of different configurations

Parameter	Capacitor clamped inverter [22]	Diode clamped inverter [22]	Cascaded H-Bridge (CHB) inverter	Proposed inverter [22]
Diodes	0	12	0	0
Capacitors	10	0	0	0
Switches	12	12	12	8
sources	6	6	3	3
Anti-parallel diodes	12	12	12	8

3. PWM TECHNIQUE

The pulse width modulation control technique has been implemented to give the gating pulse to switches. As this configuration has asymmetrical switches, a simplified PWM technique is implemented with three carriers and with one reference signal. Initially, three signals A, B, C are generated using carriers and reference signals. Signal D is taken randomly high for a positive cycle and low for a negative cycle. By using these four signals switching pulses are generated with the help of logic gates. Fig. 8 shows the switching logic and signals.

The logical notation is given in below Table-3 for getting switching pulses for each switch

Table 3. Logic gating notation

S. No	Switc h	Switching Stage
1	S1	C
2	S2	$A\overline{C}$
3	S3	$A\overline{B}$
4	S4	B
5	S5	$D + \overline{AD}$
6	S6	$\overline{D} + \overline{AD}$
7	S7	AD
8	S8	$A\overline{D}$

Schematic model of switching logic is shown in Fig. 7. Three carrier wave forms of 3500 Hz frequency are compared with a sinusoidal wave form of 50 Hz frequency to generate the pulses A, B, C and D. The pulses for switches S_1 to S_8 are generated by using logic gates.

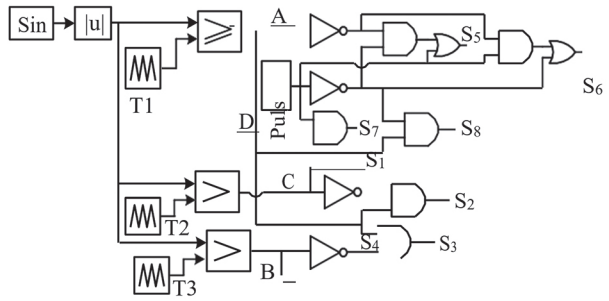


Fig. 7. Schematic model of switching logic

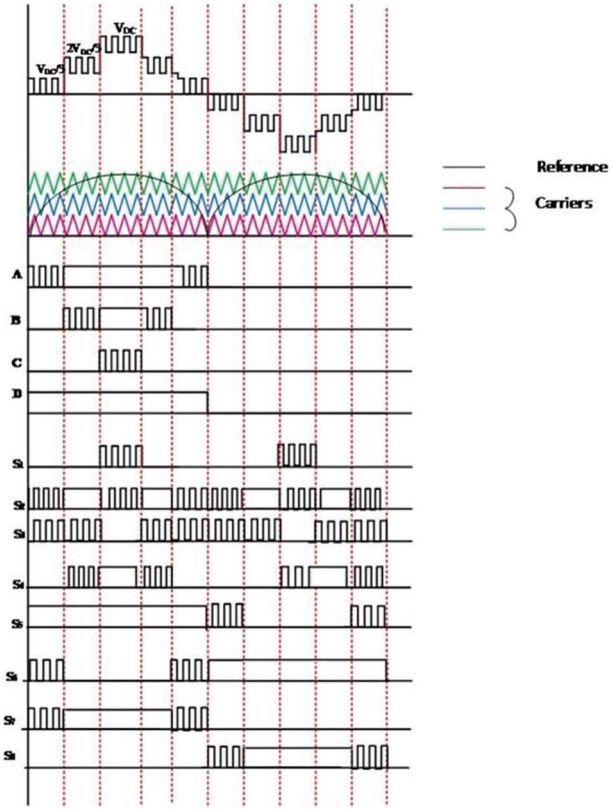


Fig. 8. PWM Technique

4. SIMULATION RESULTS

The proposed 7-level inverter was configured in MATLAB platform and implemented in Simulink. While developing a seven-level inverter, Power supply was considered as DC sources. Generally, this DC sources do not allow the currents in reverse direction or for charging. Hence, charging currents for DC sources will be required in R-L load. In the discharging mode of L. For gating pulses, Fig. 9 shows the pulses of A, B, C, and D generated by level-shifted pulse width modulation. The sinusoidal wave form is taken as a reference signal and three triangular waveforms are taken as carrier signals. By comparing this reference signal and carrier signal, pulses A, B, C are generated. Pulse D is ON for a positive half cycle and OFF for the negative half cycle.

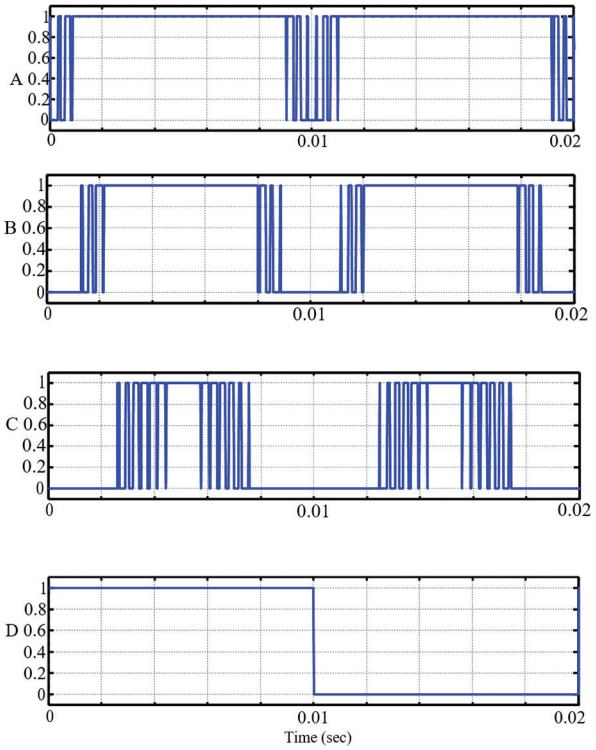
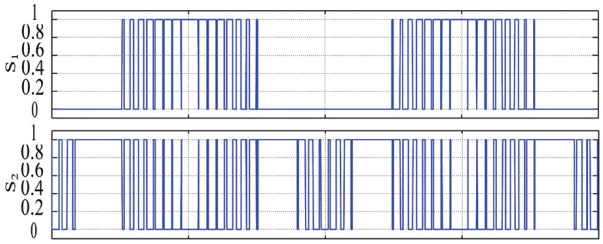


Fig. 9. PWM Pulses A, B, C and D

Fig. 10 shows the gating pulses for switches S_1 through S_8. The signals A, B, C and D are logically combined using logic gates to generate the gating pulses S_1 to S_8 as shown in Fig. 10. The same logic is implemented in MATLAB and the resulting gating pulses as shown in Fig. 12 which are same as in Fig. 10.



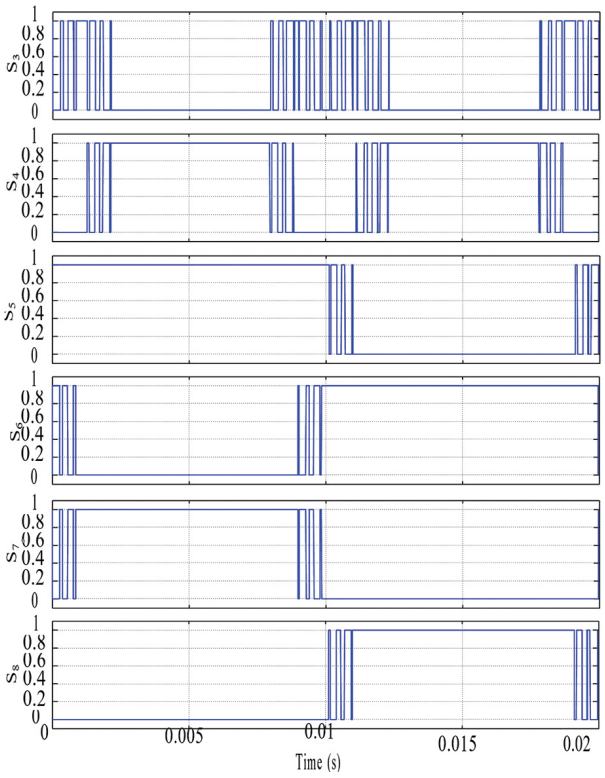


Fig. 10. Switching Pulses

Table-4 shows the Simulink circuit Parameter values.

Table 4. Simulink circuit Parameters

Parameter	Value
VDC	300 V
Load Resistance	100-ohm
Load Inductance	10 mH
Switching frequency	3500 Hz
System frequency	50 Hz
Peak Voltage	298.9 V
RMS Voltage	211.35 V
Peak Current	3.009 amp
RMS Current	2.12 amp
Filter Inductance	20 mH
Filter Capacitance	340 µF

4.1. CASE 1: R LOAD

LC filter was not considered or incorporated into the proposed inverter between load and inverter output because of testing the current THD and performance without using any filter. Hence, the current waveform will be in a similar shape as the voltage waveform with a difference in magnitude. Fig. 11 shows the seven- level PWM output voltage waveform for R-load. The magnitude of the output voltage is 300 volts and 10- ohm resistance is considered as a load. The voltage waveform and current waveforms are depicted in Fig. 11 (a) and (b) respectively. The magnitude of current will be nearly 3 amp as per system ratings.

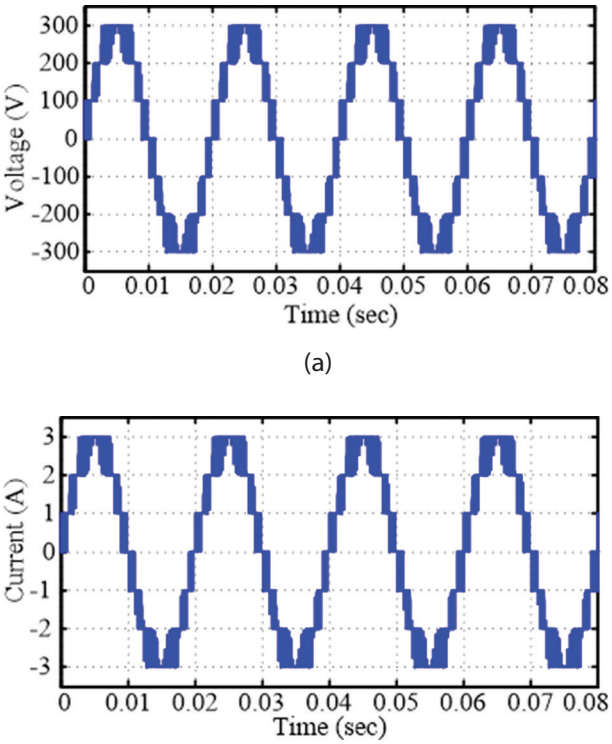
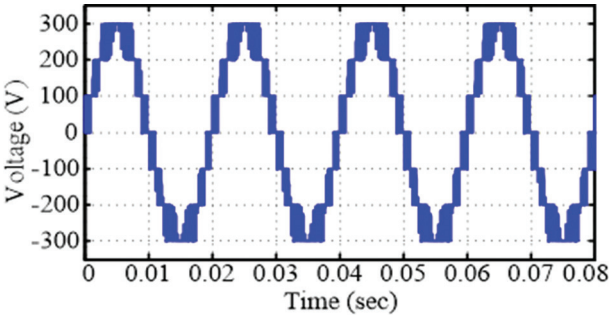
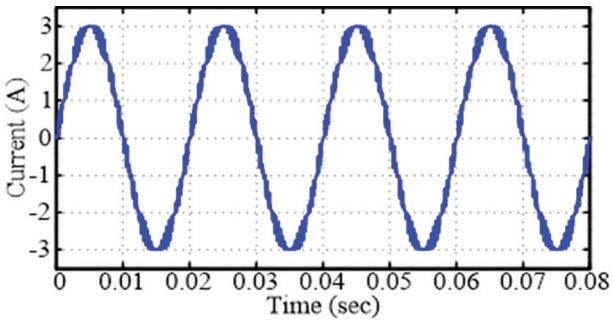


Fig. 11. Output waveforms for R load (a) Inverter output voltage (b) Load current

4.2. CASE 2: R-L LOAD

The same inverter configuration was tested for R-L load. As mentioned earlier no filter is used in this case also. However, due to load inductance, the current waveform is nearly sinusoidal. Moreover, there is no discharging path, hence there will not be any phase angle difference between voltage and current. To achieve the same magnitude of current in R load, the possible R-L is selected for comparison in THD. The voltage and current waveform for R-L load is depicted in Fig. 12 (a) and (b). Due to the absence of a filter, there will not be any significant changes in Voltage as compared to R-load. But the shape of the current is nearly sinusoidal.



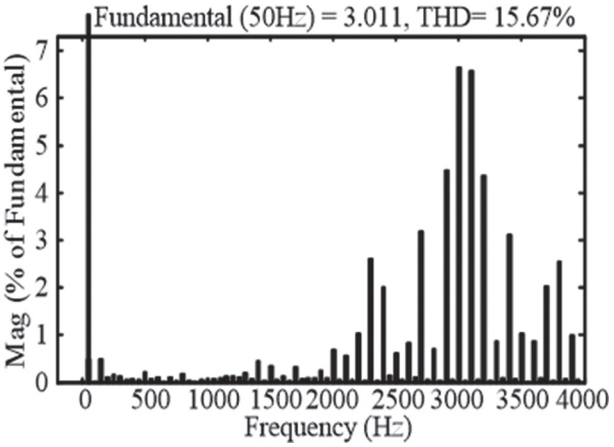


(b)

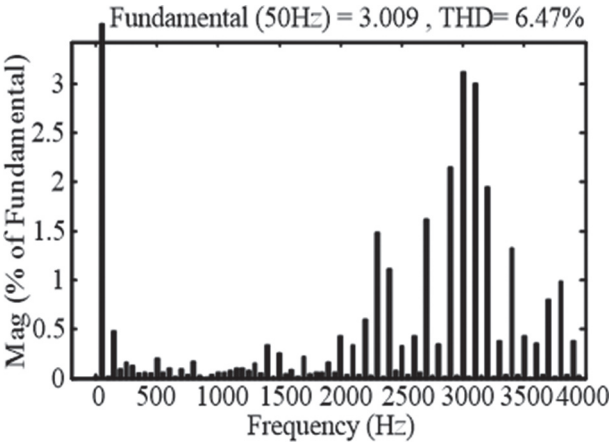
Fig. 12. Output waveforms for R-L load (a) Inverter output voltage (b) Load current

4.3. THD OF CURRENTS IN R AND R-L LOAD

The designing multilevel inverter aims to reduce THD in currents. To test the value of THD, the proposed system is designed without using any filters. For better understanding, the THDI for R load and R-L load with the same magnitude are presented in Fig. 13 (a) and (b) respectively.



(a)



(b)

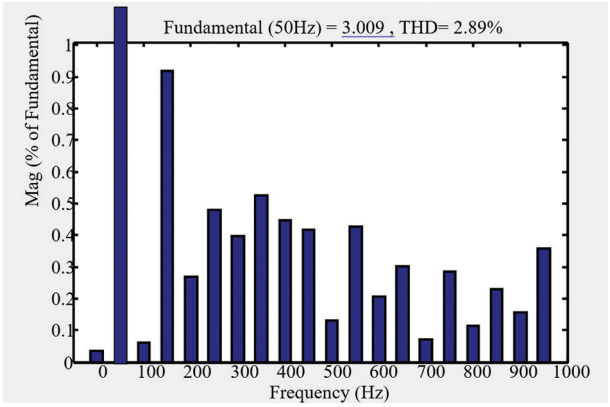
Fig. 13. FFT analysis of the current with belonging THD for (a) R load (b) R-L Load

From Fig. 13, it is clear that THD has been reduced for R-L load when compared to R-load, due to the inductance of load which acts as a filter. The lower- order harmonics are minimized, but higher-order harmonics are present. These higher-order harmonics can be minimized easily using passive filters. This will be the most benevolent feature for this proposed inverter. In general, the lower order harmonics are dangerous to the load or grid, the proposed inverter can reduce the effect of lower order harmonics and only significant magnitudes are presented in higher- order harmonics from the FFT spectrum. Further, the THDI can be minimized with a proper LC filter connected between the inverter and load.

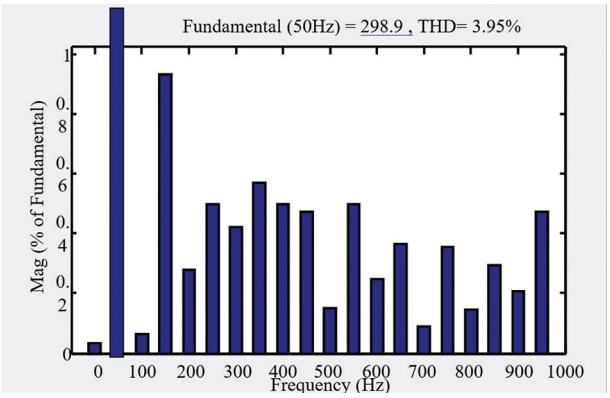
Table 5. Comparison of THDI

Parameter	Capacitor clamped inverter [22]	Diode clamped inverter [22]	Cascaded H-Bridge (CHB) inverter [22]	Proposed inverter
THDI with filter	6.8	5.7	4.9	2.9

In general, multilevel inverters are connected to load through an LC filter. Hence, the THDI and THDV for R- L load with an LC filter is shown in Fig. 14. The percentage of THDI and THDV is less than 5 percent which is allowable in the industry applications



(a)



(b)

Fig. 14. FFT analysis with belonging THD for R-L load with LC filter (a) THDI (b) THDV

5. CONCLUSION

Concludingly this is to submit that the seven-level series/parallel inverter could be implemented with a lesser number of switches and the PWM technique was applied with digital logic for this configuration. The circuit and the control logic were implemented using MATLAB software. Three voltage sources of each 100 volts were connected in series/parallel configuration using IGBT switches. The pulse width modulation technique was applied for giving the gating pulses to switches. The signals from the PWM technique were mixed by using logic gates to get the gating pulses for corresponding switches. The seven-level output voltage with the PWM technique was observed forboth R and RL loads with a magnitude of 300 volts. The current waveforms were also presented for both the loads with their THDI and THDV values. It was observed that; the effect of lower order harmonics would be reduced witha proposed inverter.

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High Efficiency, Good phase linearity 0.18 µm CMOS Power Amplifier for MBAN-UWB Applications

Original Scientific Paper

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Abstract *– This paper presents the design of 3.1-10.6 GHz class AB power amplifier (PA) suitable for medical body area network (MBAN) Ultra-Wide Band (UWB) applications in TSMC 0.18 µm technology. An optimization technique to simultaneously maximize power added efficiency(PAE) and minimize group delay variation is employed. Source and Load-pull contours are used to design inter and output stage matching circuits. The post-layout simulation results indicated that the designed PA has a maximum PAE of 32 % and an output 1-dB compression of 11 dBm at 4 GHz. In addition, a small group delay variation of ± 50 ps was realized over the whole required frequency band . Moreover, the proposed PA has small signal power gain (S21) of 12.5 dB with ripple less than 1.5 dB over the frequency range between 3.1 GHz to 10.6 GHz, while consuming 36 mW.*

Keywords *– Group Delay (GD); Medical Body Area Network (MBAN); Ultra-Wide Band (UWB); Power Added Efficiency (PAE); Class AB, Power Amplifier (PA)*

1. INTRODUCTION

Tremendous development in healthcare electronics system based on the Radio Frequency (RF) CMOS technology has a great impact in the industry of bio-medical to enhance the diagnosis and health monitoring. Medical body area network (MBAN) can be defined as a wireless network consisting of small intelligent devices that can be attached to the human body surface or implanted inside the body that act as MBAN nodes for remote sensing and diagnosis [1]. The Federal Communications Commission (FCC) defined the ultra-wide band signal as the signal whose bandwidth is more than five hundred megahertz or fractional bandwidth bigger than 20% and specified the spectrum from 3.1 to 10.6 GHz for UWB applications [2]. High data rate transmission of UWB systems qualifies them to be a promising candidate for MBAN applications in real time monitoring of multi-node systems [3]. In 2012, the IEEE LAN/MAN standards committee released the IEEE 802.15.6 standard that explains the detailing of different Physical (PHY) layers for Ultra-Wideband (UWB) and Human Body Communications (HBC) layers for MBAN [4]. The objective of this standard was to develop a short-range wireless communication system for low power devices positioned around, or implanted inside the human body [3]. In this standard, As seen in Fig. 1, the 3.1 -10.6 GHz spectrum is divided into low band of three channels (channels 0-2) and high band of eight channel (channels 3–10). Each channel has a bandwidth of 499.2 MHz to achieve data rates for transmissions up to 480 Mb/s [4].

Some issues for CMOS technology such as [5] substrate coupling, poor quality factor of the on-chip passives, hot carrier effect and small oxide breakdown voltage of CMOS make the design of CMOS UWB power amplifiers a difficult and challenging task. It is required for the UWB PAs to have broadband matching, flat gain over the desired bandwidth, good linearity, small group delay, and acceptable PAE. The CMOS UWB-PAs presented in literature adopt different topologies and operate over different bands such as 3.0 to 5.0 GHz, and 6.0 GHz to 10.0 GHz [6] – [25].

The resistive shunt feedback topology [6]-[8] achieves wideband matching and better gain flatness over wide bandwidth, but suffers from its small PAE and consumes large DC power consumption. Also, the distributed amplifiers provide a good wideband matching and broad gain-bandwidth. However, it consumes large area and dissipates high DC power that re-

duces the PAE [9]. Meanwhile, the traditional common source (CS) and cascode with inductive degeneration topology provides good gain and noise performance. However, the matching is not as good as resistive shunt feedback topology [10-12]. Whereas, the current reuse structure, compared to cascode and CS structure, offers better isolation and larger gain thanks to its higher output impedance and smaller miller capacitance [13-17]. However, its main drawback is the bad input matching.

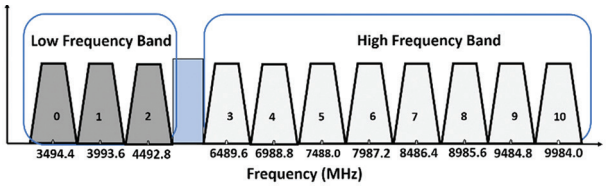


Fig. 1. UWB-MBAN operating frequency bands.

In the design of UWB systems with impulse response, it is necessary to keep the group delay (GD) constant over the whole frequency range of interest in order to avoid signal distortion. Through literature, different techniques are reported to overcome the group delay issues in the UWB PAs. The authors in [18] presented a negative group delay circuit to reduce the group delay variation in UWB InGaP/GaAs HBT MMIC amplifier. But utilizing additional negative GD circuit consumes large area and deteriorate the PAE significantly. Another technique by optimizing the value of inductors is presented in [19] but, also, it improves the GD at the expense of the reduction in PAE. Recently, David. et.al [21] improved the group delay variation using s a stacked FET structure, However, the stacked FET requires high supply voltage and should be accurately biased to avoid transistors breakdown. Generally, the PAE is important in the design of UWB-PAs as it measures the effectiveness of converting the DC power to RF output power. Therefore, a trade-off between design requirements remains existing: For example, broad bandwidth may lead to a degradation in group delay variation and PAE.

In this paper, a minimum group delay variation, well matched CMOS PA covering the frequency range from 3.1 GHz to 10.6 GHz, with a high PAE for a MBAN-UWB transmitter is designed and simulated using 0.18 µm CMOS Technology. The proposed design consists of two stages; the first diver stage is a common gate (CG) amplifier loaded with a diode connected transistor in series with a small inductor for gain maximization, and the second power stage is designed to maximize the PAE using a simple CS amplifier with series and shunt peaking inductive load to enlarge the operating bandwidth.

The remainder of this paper is organized as follows: the UWB designed PA circuit is described in section two. Section three discusses the methodology for improving the power added efficiency and group delay performance. Post layout simulation results and comparison to recently published PAs are reported in section four. Finally, the conclusion of this paper is presented in section five.

2. TWO-STAGE PA SCHEMATIC DESCRIPTION

Fig. 2(a) and (b) show the schematic and the small signal equivalent circuit of the designed UWB PA. The proposed wideband PA made up of two stages, the first stage consists of common gate (CG) driver stage while the second stage is a common source (CS) power stage with degeneration inductor Ls3 to further improve the linearity.

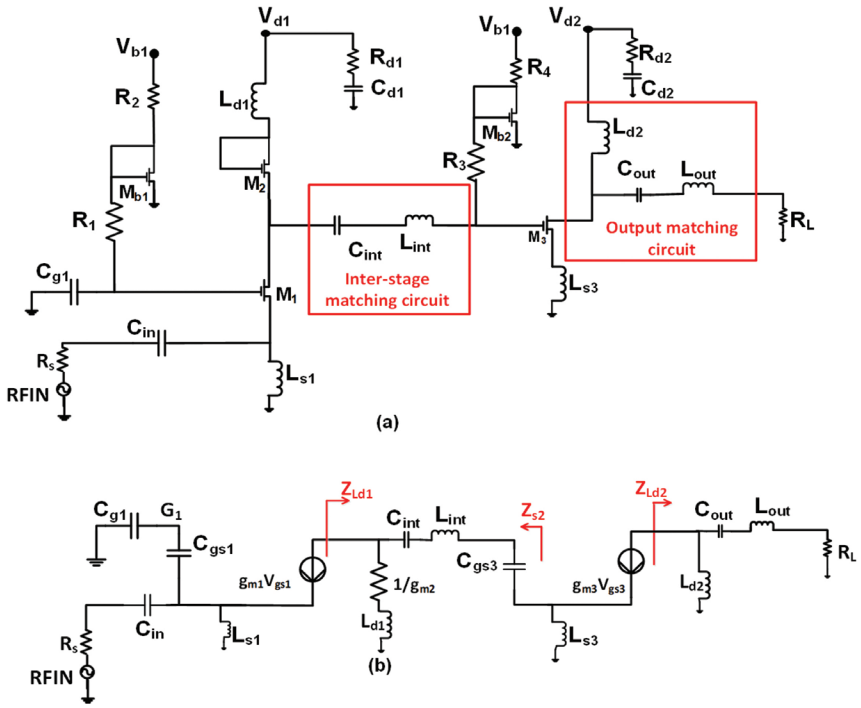


Fig. 2. (a)Circuit schematic of the designed PA (b) Small-signal equivalent circuit the designed PA.

The proposed PA is initially targeted to consume 36 mW from 2 V supply, which needs drain current of 18 mA to be divided between the two stages. *The* M_{b1}, R_1, R_2, M_{b2}, R_3 and R_4 form current mirrors that adjust the bias for transistors M_1 and M_3. The CG driver stage provides superior broadband input matching and Eq.1 expresses the input impedance of the proposed PA:

$$Z_{in} = \frac{sL_{s1}}{1 + sL_{s1}(g_{m1} + sC_{gs1})} \quad (1)$$

where g_{m1} is the transconductance of the input transistor M_1. Source inductor L_{s1} and the size of transistor M_1 are optimized to cancel the imaginary part of Eq.1 leaving the 50-ohm real input impedance [26]-[28]. In addition, compared to the CS configuration, the CG provides better isolation as there is no miller capacitance at the input and better noise performance as the gate is bypassed to ground leading to the absence of the gate noise current. To maximize the gain of the first stage, a large inductive load is required at the drain of transistor M_2. However, this large inductor will have small resonance frequency that will affect the gain flatness largely. Therefore, a diode connected transistor M_2 in series with a small drain inductor L_{d1} are utilized acting as the inductive load of the first stage which will save the area and improve the linearity while achieving reasonable flattened gain over the whole band. Fig.3 compares the effect of employing large load inductor alone or using the diode connected load in series with small load inductor on the gain flatness which indicates the enhancement of the 3-dB bandwidth by using the diode connected load.

The amplified signal from the common gate transistor M_1 is moved toward the second stage using the interstage matching composed of MIM capacitor C_{int}, large inductor L_{int} and the gate to source parasitic capacitance C_{gs3}. The Inter-stage matching is important to enhance gain flatness and at the same time affects the group delay and PAE greatly as will be discussed in section 3.

The 2nd stage consists of a CS amplifier which is designed to be biased for operation in class AB to trade-off efficiency and linearity. Fig. 4 shows the I-V wave forms of M_3 at 7 GHz with -5 dBm input power indicating class AB operation. The L_{d2} and L_{out} are exploited as a shunt and series peaking load for the second stage to realize wide flattened gain, little group delay variation and high PAE.

To realize the wide and flat gain response across the 3.1- 10.6 GHz band, a staggered tuning technique is utilized concurrently with better optimization of the value of the interstage inductor L_{int} to move away the tuning center frequency of each stage by a value related to its 3-dB bandwidth [25]. The tuning frequency can be defined by optimizing the sizes of transistors M_1 and M_3 which control to the current-gain cut-off frequencies $\omega_T = g_m/C_{gs}$, where, g_m and C_{gs} are the transconductance and gate-source capacitance, respectively. The size of the common source transistor M_3 of the second stage should be maximized to enhance the output power and power added efficiency. Therefore, only the size of M_1 and the value of the interstage inductor L_{int} are optimized to increase the gain- bandwidth. Fig.5 shows the effect of varying the interstage inductor L_{int} and the size of transistor M_1 on realizing wide and flat power gain.

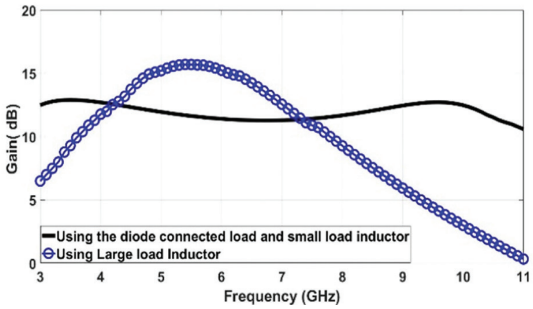


Fig. 3. Effect of employing large load inductor alone or using the diode connected load in series with small load inductor on the gain flatness.

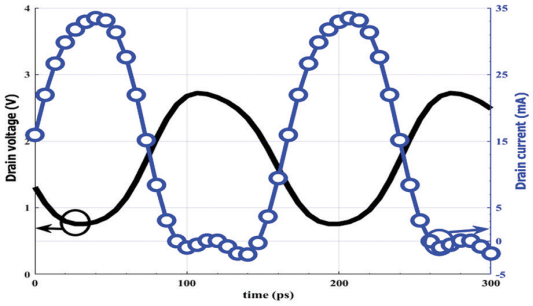


Fig. 4. The current and voltage behavior at 7 GHz for class AB PA at -5 dBm input power.

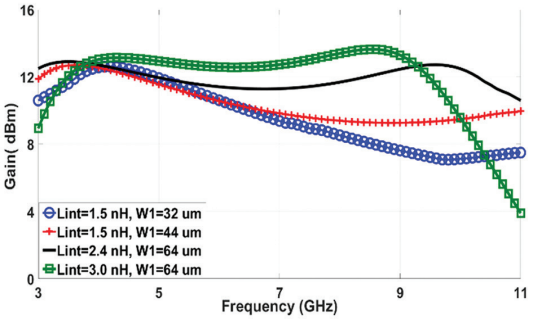


Fig. 5. Influence of changing the value of L_{int} and width of M_1 on realizing wide and flat gain.

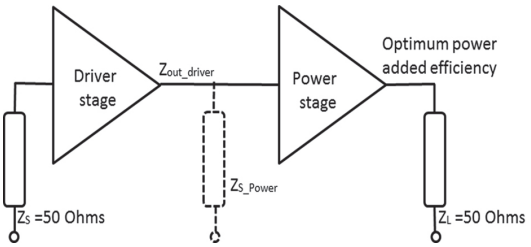


Fig. 6. Two stage power amplifiers.

3. DESIGN ANALYSIS

3.1. SOURCE AND LOAD PULL ANALYSIS

In the two-stages amplifier design as shown in Fig. 6, the output impedance of the driver amplifier (Zout_driver) is the source impedance (Zs_power) seen by the power stage. For studying the result of changing the source impedance of the second stage on the PAE, constant PAE contours are drawn in the Smith Chart, with changing source impedance using the Advanced Design System (ADS). The input signal level is fixed at -5 dBm for operation in the linear region and the load impedance is set to 50 ohms, while the impedance of the source was being changed. The constant power added efficiency contours at 4 and 8 GHz for various source impedances are shown at Fig. 7(a). As presented in Fig. 7(a), the source impedance that realize maximum PAE is existed in the inductive area of the Smith Chart. Therefore, an inter-stage matching circuit created by inductor L_{int} and capacitor $C_{int.}$ is designed and optimized to make the output impedance of the driver stage to agree with the points of maximum power added efficiency in source-pull contours of the power stage shown in Fig.7(a). Using the small signal equivalent circuit at Fig. 2(b), the output impedance of the first stage can be expressed by Eq.2:

$$Z_{out1}(s) = Z_{s2} = \frac{s^2(L_{int}+L_{d1})C_{int}g_{m2} + SC_{int} + g_{m2}}{SC_{int}g_{m2}} \quad (2)$$

As Inductor L_{int} has a fundamental role in the design of interstage matching circuit, it is optimized for maximizing the PAE, in addition to, taking into consideration gain flatness, group delay variation, chip size and input / output impedance matching.

Using the load-pull simulation in ADS and following similar steps, we can search for the optimum load location on Smith Chart which maximizes the PAE over the whole band. Fig. 7(b) reports the constant PAE contours on Smith Chart at 4, and 8 GHz using various load impedances for the second stage PA while the source impedance is fixed with the optimum impedance from the source-pull simulation.

The load impedance of the designed PA after adding the output matching can be written as:

$$Z_{Ld2}(s) = sL_{d2} \,\|\, \left(\frac{s^2L_{out}C_{out}+1}{sC_{out}} + R_L\right) \quad (3)$$

The output matching circuit is made up of the series peaking inductor L_{out} and shunt peaking inductor L_{d2} to match the load impedance Z_{ld2} with the load-pull contours at Fig.7(b) for maximum PAE.

Based on the prior description, L_{int}, L_{out} and L_{d2} affects the PAE significantly. Hence Fig. 8 presents the Influence of changing their values on realizing high PAE.

3.2. GROUP DELAY

Group delay (GD) is utilized as an effective test for signal distortion and can be calculated by taking the derivative transfer function phase with respect to angular frequency. A simplified formula for the overall transfer function H(s) and group delay can be expressed by Eq.4, Eq.5 and Eq.6.

$$H(s) = |H(j\omega)|e^{j\theta(\omega)} = -\frac{g_{m1}g_{m3}SL_{eq}(1 + Sg_{m2}L_{d1})}{S^2C_{eq}g_{m2}(L_{int}+L_{d1}) + SC_{eq} + g_{m2}} \quad (4)$$

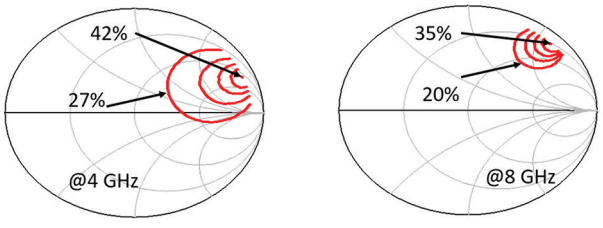
Where $C_{eq} = \frac{C_{\text{int}}C_{gs3}}{C_{\text{int}}+C_{gs3}}$ and $L_{eq} = \frac{L_{\text{d2}}L_{\text{ser}}}{L_{\text{d2}}+L_{\text{ser}}}$

$$G_D(\omega) = -\frac{\partial(\theta(\omega))}{\partial\omega} \quad (5)$$

After simplification and guided by ref [16];

$$G_D(\omega) \simeq -\frac{L_{int} + \frac{1}{\omega^2C_{gs3}}}{\frac{(1+Sg_{m2}L_{d1})}{g_{m2}} + \frac{g_{m2}}{(1+Sg_{m2}L_{d1})}\left(L_{int}\omega - \frac{1}{\omega C_{gs3}}\right)^2} \quad (6)$$

Based on the derived formula of the GD presented in Eq.6 and circuit simulation at Fig.9, Inductor L_{int} has a great effect on the GD variation where increasing its value will improve the GD performance. However, larger value of L_{int} will reduce the 3-dB bandwidth largely as concluded from Fig.5. Therefore, according to the previous explanation and guided by Fig. 5, 8, and 9, Inductors L_{int}, L_{out} and L_{d2}, in addition to the sizes of transistor M_1 and M_2, have large effect on the gain- bandwidth, PAE and group delay. For example, increasing the size of L_{int} will improve the PAE and GD variation at the expense on a reduction on the 3-dB bandwidth. Therefore, we have concurrently optimized their values to improve PAE, minimize GD variations and realize wide flattened gain simultaneously. After many optimization trials, the values of L_{int}, L_{out} and L_{d2}, are optimized and selected to be 2.8 nH, 0.46 nH, and 3 nH, respectively after EM simulation is performed.



(a)

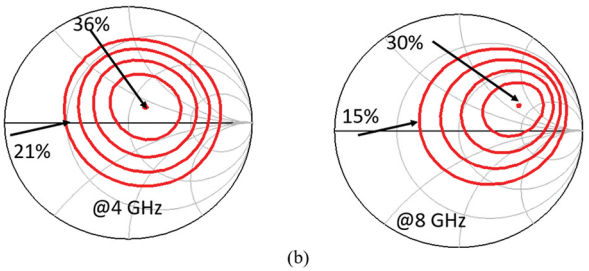


Fig. 7. (a) Constant PAE contours in 3% step at 4and 8 GHz for varying source impedance of 2nd stage. **(b)** Constant PAE contours in 3% step at 4 and 8 GHz for varying load impedance of 2nd stage.

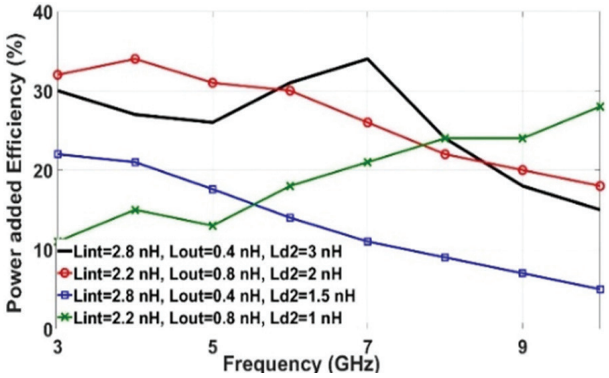


Fig. 8. Influence of changing the value of L_{int}, L_{out} and L_{d2} on the maximum PAE over the 3-10 GHz band.

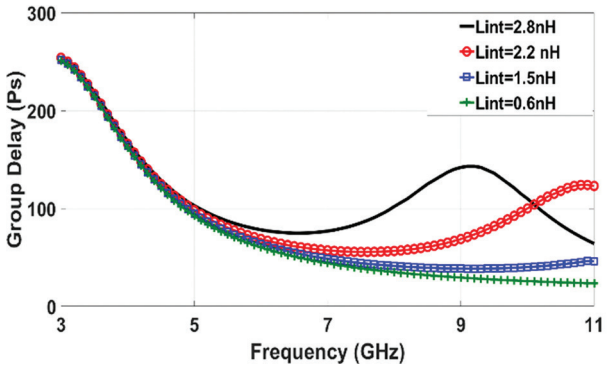


Fig. 9. Influence of changing the value of L_{int} on realizing small GD variations.

4. POST-LAYOUT SIMULATION RESULTS

The proposed UWB-PA has been designed and simulated in TSMC 0.18 µm CMOS technology. The layout of the PA is shown in Fig. 10 with size of 0.55 mm^2 including the measurement pads.

A. Pre and post layout simulated S-parameters:

Fig. 11 and Fig. 12 show the correspondence between the pre-and post-layout S-parameters using Cadence Spectre. As presented in Fig. 11, an average small signal gain($|S_{21}|$) of 12.5 ±1.5 dB and reverse isolation ($|S_{12}|$) better than -25 dB are achieved over the 3.1 to 10.6 GHz. Furthermore, a post-layout input return loss ($|S_{11}|$) and output return loss ($|S_{22}|$) less than -4.5 dB and -8.5 dB, respectively are realized also over the frequency of interest as illustrated in Fig.12.The wideband matching of the designed PA enhance the PAE and improve the GD vatiations.

B. Large Signal Simulations (Output 1dB compression point and PAE)

The harmonic balance simulation is used to test the large signal performance across the required frequency band. As shown in Fig.13 The maximum achieved PAE by the designed PA at 4 GHz, 7 GHz and 9 GHz are 32.5%, 20% and 18%, respectively. Besides that, the designed UWB-PA achieved output 1-dB compression points of, 11, 6 and 3.5 dBm and saturated output power of, 13, 11.5, and 10 dBm, at 4, 7 and 9 GHz, respectively as illustrated in Figure 14.

C. Group delay, DC power and stability:

As shown in Fig. 15, good post-layout simulated phase linearity (i.e., small group delay variation) of ±50 ps is achieved over the targeted frequency. In addition, the stability factor of the designed PA is greater than one, demonstrating that it is uncondionally stable over a wide frequency band from 0.5 GHz to 16 GHz as shown in Fig.16. In normal biasing conditions, the PA consumes 36 mW from 2 V supply.

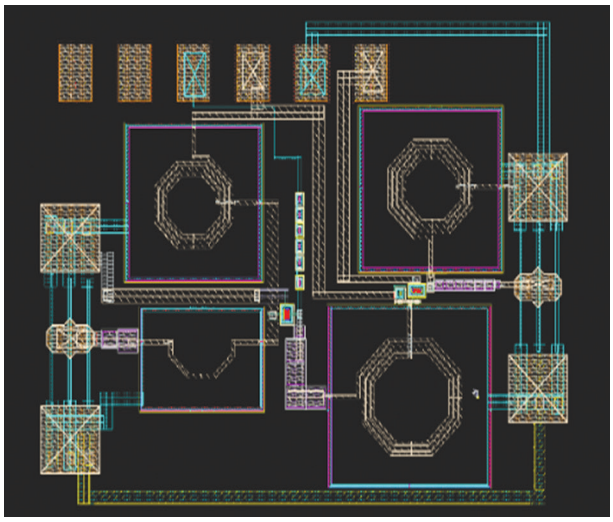


Fig. 10. Layout of the designed two-stage PA.

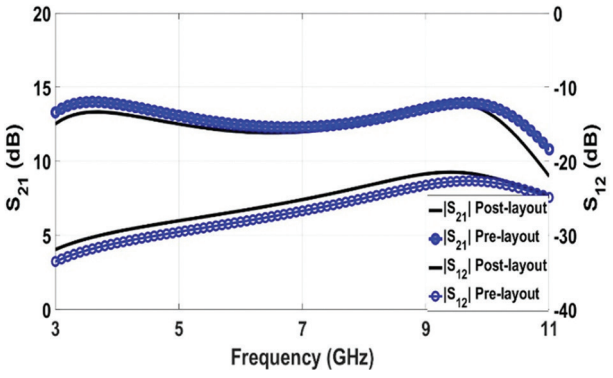


Fig. 11. Pre- and post-layout power gain ($|S_{21}|$) and reverse isolation ($|S_{12}|$) of the suggested UWB-PA.

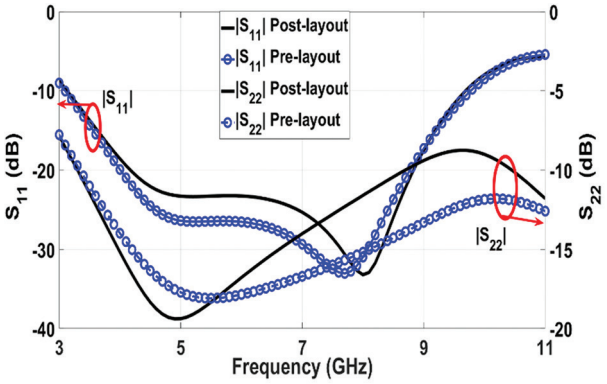


Fig. 12. Pre- and post-layout output return loss ($|S_{22}|$) and input return loss ($|S_{11}|$) of the suggested UWB-PA.

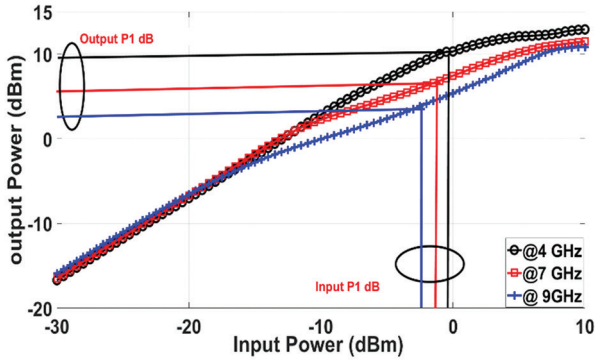


Fig. 14. Post-layout simulation result of the output power versus input power of the suggested UWB-PA.

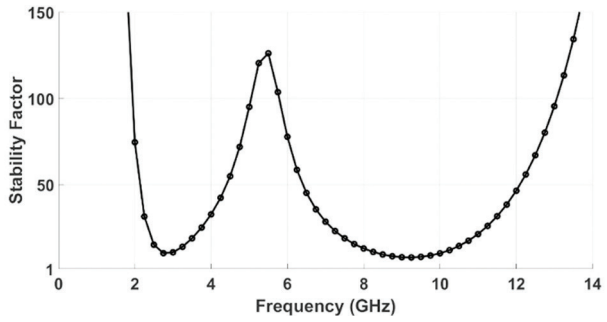


Fig. 16. Stability factor of the proposed PA.

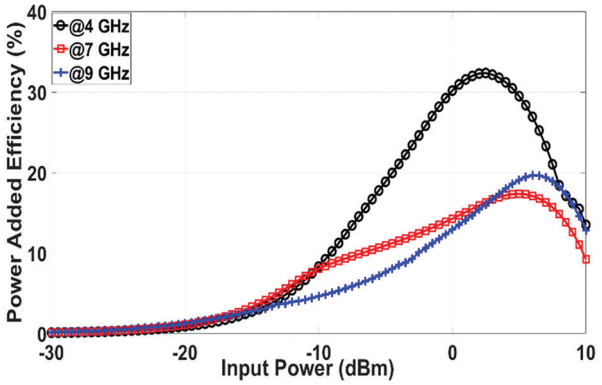


Fig. 13. Post-layout simulation result of PAE versus RF input power of the suggested UWB-PA.

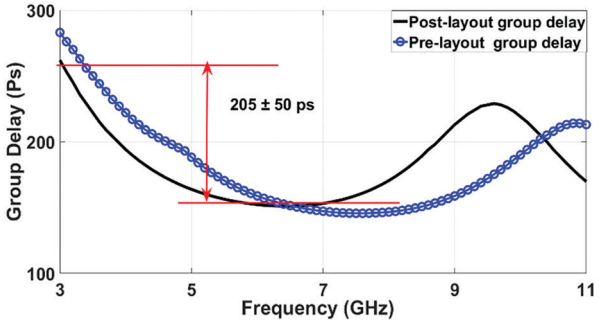


Fig. 15. Pre- and post-layout Simulation of GD variation of the suggested UWB-PA.

Table I summarizes the post-layout simulation results of the desinged PA and compares it's performance with the recently published UWB amplifers. Our proposed PA has good matching and gain flattness behaviour over the whole bandwidth, while providing high PAE and small group delay variation.

Moreover, the FOM[22, 29], given by Eq. 7, presents that the the proposed PA has a competitive performance compared to previous art.

$$FOM = \left(\frac{10^{Pout/10}}{1000}\right) * 10^{\frac{Gain}{10}} * F^2 * PAE \quad (7)$$

Table 1. Comparison of the designed PA post-layout simulation results with different published 0.18 µm CMOS UWB-PAs.

Ref.	CMOS Tech,	Freq. (GH)	S11 (dB)	S22 (dB)	Gain (dB)	GD (ps)	Max. PAE (%)	OP1dB (dBm)	Area (mm2)	DC Power	FOM
[6] 2021	45 nm	3.1-10.6	<-10	<-10	45± 0.5	NA	NA	10 @ 7 GHz	0.8	125	NA
[7] * 2019	130 nm	8-12	<-8	<-7	10	NA	29 @10 GHz	13@ 10 GHz	NA	20	578
[8] * 2015	180 nm	3.1-10.6	<-15	<-8	10	NA	10 @7 GHz	3 @ 7 GHz	0.9	15	10
[11] 2015	110 nm	8-12	<-5	<-7	9± 1.5	NA	20 @ 10 GHz	9 @ 10 GHz	0.66	NA	150
[12]* 2014	180 nm	3-5	<-7	<-8	13.3±1	NA	15 @ 4 GHz	1.5 @ 4 GHz	NA	25	12
[13] * 2013	180 nm	5-9	<-4	<-5	16±1	±20	13 @ 5 GHz	3 @ 5 GHz	0.6	25	33
[14] 2015	180 nm	5-10.6	<-5.5	<-7	14±1	±40	10 @ 8 GHz	3 @ 8 GHz	0.77	20	41

[15] * 2012	180 nm	5-11	<-9	<-9	11.5± 1	±41	18 @ 7 GHz	3.7 @ 7 GHz	0.96	18	44
[16] 2019	180 nm	3-10	<-8.5	<-10	11.5± 0.8	±68	26 @ 7 GHz	9 @ 7 GHz	0.8	34	156
[17] *2018	180 nm	3.1-10.6	<-6	<-7	15± 1	NA	22 @ 6 GHz	4 @ 6 GHz	0.53	15	80
[19] 2012	180 nm	3-10	<-9	<-13	11± 0.8	±85	NA	5 @ 6 GHz	0.77	100	NA
[21] 2017	65 nm	3-10	<-7	<-9	11± 2	±22	18 @ 6 GHz	15 @ 6 GHz	0.94	100	324
[22] 2018	180 nm	1.5-5	<-2	<-5	17±3	NA	22 @ 4 GHz	7 @ 4 GHz	1.2	25	140
[23] 2018	130 nm	6-9	<-8	<-9	9± 1	NA	22 @ 7 GHz	7 @ 7 GHz	0.86	24	56
[24] 2021	130 nm	7.8-11.5	<-9	<-5	8± 1	NA	20 @ 9 GHz	12 @ 9 GHz	1.1	58	162
This work*	180 nm	3.1- 10.6	<-4.5	<-8.5	12.5 ± 1.5	±50	32.5 @ 4 GHz	11 @ 9 GHz	0.55	36	165

*Simulated

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Performance evaluation and implementations of MFCC, SVM and MLP algorithms in the FPGA board

Original Scientific Paper

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Abstract *– One of the most difficult speech recognition tasks is accurate recognition of human-to-human communication. Advances in deep learning over the last few years have produced major speech improvements in recognition on the representative Switch-board conversational corpus. Word error rates that just a few years ago were 14% have dropped to 8.0%, then 6.6% and most recently 5.8%, and are now believed to be within striking range of human performance. This raises two issues - what is human performance, and how far down can we still drive speech recognition error rates? The main objective of this article is the development of a comparative study of the performance of Automatic Speech Recognition (ASR) algorithms using a database made up of a set of signals created by female and male speakers of different ages. We will also develop techniques for the Software and Hardware implementation of these algorithms and test them in an embedded electronic card based on a reconfigurable circuit (Field Programmable Gate Array FPGA). We will present an analysis of the results of classifications for the best Support Vector Machine architectures (SVM) and Artificial Neural Networks of Multi-Layer Perceptron (MLP). Following our analysis, we created NIOSII processors and we tested their operations as well as their characteristics. The characteristics of each processor are specified in this article (cost, size, speed, power consumption and complexity). At the end of this work, we physically implemented the architecture of the Mel Frequency Cepstral Coefficients (MFCC) extraction algorithm as well as the classification algorithm that provided the best results.*

Keywords *– Automatic speech recognition, Real time, SVM, MLP, ANN, MFCC, FPGA.*

1. INTRODUCTION

Automatic speech recognition is a computer technique that analyzes speech picked up by a microphone and transcribes it into machine-readable text. The first speech recognition system was created in 1952 [1]. This electronic system, developed by Davis, Biddulph and Balashek at Bell Labs [2], was essentially composed of relays and its performance was limited to recognizing isolated digits [1]. Research has been then considerably increased during the 1970s by IBM (1972-1993). Nowadays, speech recognition is related to many different areas of science: automatic language processing, linguistics, information theory, signal processing, neural networks, artificial intelligence, etc. In the field of speech processing, most algorithms require more complex mathematical operations and a very rich database. This field also requires the use of fast electronic circuits, reconfigurable for the training phase and capable of manipulating large amounts of information generated by the audio source. The main objective of this paper is to develop techniques for the software and hardware implementation of speech recognition algorithms and to compare these performances.

In the first part of our study, we propose two methods to design a robotic system capable of communicating with users. The first method is intended for the task of pre-processing (extraction of audio signals) and the second one consists in performing the task of speech recognition of the audio signal just after the extraction of the useful signal. The algorithms proposed to design this system are the MFCC algorithm for extracting the speech signals, and the Support Vector Machine (SVM) and Artificial Neural Network (ANN) algorithms for the classification of the speech signals of the names of teachers in our institution obtained after the MFCC extraction.

The objective of this work is the evaluation of performance (strengths and limitations encountered during the use of such a model) between ANN of type MLP and SVM (one against all and one against one) in the field of speech recognition. The three algorithms mentioned above require a very fast processor to perform the tasks of processing, coding, extraction and recognition. The second Part presented in this paper is limited to the chain of audio signal acquisition, processing and restitution of an audio signal provided by a microphone. We will also show how to implement an electronic system called NIOSII capable of processing audio signals on the DE2-70 FPGA (*Field Programmable Gate Array*) board. We have proposed this version of the new generation of reconfigurable embedded processors, which can be created by modifying the internal structure of the FPGA circuit to implement the algorithms studied in part 1. At the end of this work, we compared our implementation with traditional digital implementations [3], [4] and [5].

2. WORK LITERATURE REVIEW

In this part, we will point out some references who have treated subjects approaching the hardware and / or software implementations of object recognition algorithms in general and speech recognition in particular. They are based on classical methods for hardware implementation.

The study discussed in [6] demonstrated an HMM-free approach to training a speech recognizer which uses a neural network to directly predict transcript characters given the audio of an utterance. This approach discards many of the assumptions considered in modern HMM-based LVCSR systems in favor of treating speech recognition as a direct sequence transduction problem. The approach trains a neural network using the connectionist temporal classification (CTC) loss function, which amounts to maximizing the likelihood of an output sequence by efficiently summing over all possible input-output sequence alignments. Using CTC the authors were able to train a neural network to predict the character sequence of test utterances with a character error rate (CER) under 10% on the Wall Street Journal LVCSR corpus. While impressive in its own right, these results are not yet 1 competitive with existing HMM-based systems in terms of word error rate (WER).

In [7], the authors gave an overview of the hardware architectures of reconfigurable computing machines, and the software that targets these machines, such as compilation tools. They described two main methods of traditional computer science for running algorithms. The first is to use an application specific integrated circuit, or ASIC, to perform operations in the hardware. Because these ASICs are designed specifically to perform a given calculation, they are very fast and efficient when performing the exact calculation for which they were designed.

The study established in [8] describes an implementation of an ANN based on the FPGA circuit, of the FAST architecture (Flexible Topology Adaptable-Size), an artificial neural network (ANN) which dynamically adapts its size. Most ANN models base their ability to adapt to problems on changing the strength of the interconnections between computational elements based to a given learning algorithm. However, constrained interconnection structures can limit this capacity. Programmable Peripherals, are very well suited to the implementation of ANNs with an adaptation circuit structure. To achieve this implementation, in this study they authors used a network of Labomat-3 (a reconfigurable platform developed in their lab), which communicates with each other using TCP / IP or a hardware connection.

In 2005 D. Verstracten et al. [9] used an analog neuron to build an RC (reservoir computing) system on FPGA, using stochastic neurons which communicate using random bit streams instead of fixed-point values. This greatly simplified the hardware implementation of arithmetic operations such as addition, non-linearity, and multiplication.

In 2002, SJ Melnikoff et al. [10], investigated the FPGA efficiency to implement a decoder based on Continuous Hidden Markov Models (HMM) representing monophones, and demonstrated that it can process speech 75 times in real time. Recurrent neural networks are generally difficult to use because there is no practical learning program. In [11], a recursive learning scheme for recurrent neural networks has been developed based on simultaneous disturbance method. Unlike ordinary correlation learning, this method is applicable to analog learning and learning of oscillatory solutions of recurrent neural networks. They physically implemented Hopfield neural networks using an FPGA.

In [12], the authors showed mathematical basis of stochastic neurons as well as specific circuits necessary to implement the processing of each neuron. They also proposed a new methodology to reproduce the nonlinear activation function. Special MATLAB toolkits are used in this work for the training and execution of neural networks [13].

In [14] the authors proposed a new hardware / software system for the implementation of ANN with two hidden layers. The first layer has three neurons and the second has two neurons, and an output layer has two neurons. Learning ANN is done using MATLAB software (the design of ANN in Simulink). The hardware synthesis of the proposed algorithm, is performed by the Generator System. Routing and implementation are done on Spartan2E type FPGAs.

In [15] a novel design for a hyperbolic tangent activation function (Tanh) has been proposed to be used in memristor-based neuromorphic architectures. The purpose of the implementation of a CMOS-based design for Tanh is to decrease power dissipation and area usage. This design also increases the overall speed of computations in ANNs, while keeping the accuracy in an acceptable range.

Another big theme in semi-supervised learning is consistency [16], [17]. In this line of research, a consistency-based task that can be trained on unlabeled data is introduced and used to pre-train networks so that they can learn a good representation of the data. These networks are in turn fine-tuned on supervised data [18], [19].

In this article we will demonstrate the advantages of our hardware implementation based on a new generation of reconfigurable processors based on FPGAs with old implementations.

3. MEL FREQUENCY CEPSTRAL COEFFICIENTS ALGORITHM (MFCC), SVM AND ARTIFICIAL NEURAL NETWORKS (ANN):

Each model of speech recognition has advantages and disadvantages. In this part, we will summarize the strengths and limitations encountered while using such a model in ASR [15], [20].

GMM (Gaussians Mixture Model):

Advantages:

- The use of a mixture of several multi-dimensional Gaussian densities allows to give a very good representation of the acoustic vectors.
- The use of the GMM model allows to accurately estimate random probability densities such as that of the acoustic vectors.
- The learning time is relatively small compared to other models such as the HMM model.

Disadvantages:

- Although they are capable of capturing a speaker's longer-term information, they do not contain dynamic aspects. For a good modeling (i.e. a lot of Gaussians) require a lot of data.

DTW (dynamic time waping):

Advantages:

The DTW algorithm is fast, well adapted to speech because it is able to take into account the temporal variations of the signal. It does not require a lot of data to run and function properly.

Disadvantages:

- DTW is very sensitive to signal segmentation. Indeed, if the starting point of the dynamic calculation is not good, the algorithm can quickly deviate from the optimum path.

HMM (Hidden Markov Model):

Advantages:

- This technology offers powerful algorithms for learning and recognition, thanks to which HMMs have been shown to be best adapted to speech recognition problems.

Disadvantages:

- Hidden Markov models present certain limitations and difficulties, which lie mainly in the choice of a good initial model for learning, that is generally random and often leads to a local optimum.

SVM (Support Vector Machines):

Advantages:

- The big advantage, over other techniques, is the ability to generalize the classification. -This method is suitable for applications with a large intra-class variation.
- SVMs have a more efficient behavior for a very small training set.

Disadvantages:

- The disadvantage of SVMs is the empirical choice of the kernel function suited to the problem.
- A second drawback is the computation time which increases as a cubic function of the number of data to be processed.

ANN (Artificial Neural Network):

Advantages:

- Neural networks are useful for the classification of static patterns.

Disadvantages:

- Neural networks cannot model long term time evolution.
- Neural networks cannot model long-term temporal evolution. They are therefore poorly adapted to the processing of sequential signals such as speech.

In the following section, we will study the SVM Support Vector Machines and the MLP Neural Network, as well as the problem of classification when we have several classes. Finally, we have implemented and tested the MLP and SVM by NIOSII processors created in the FPGA board for the speech recognition application.

3.1. EXTRACTION OF VOICE SIGNALS AND CREATION OF A DATABASE BY THE MFCC ALGORITHM:

In our study, we used the MFCC speech signal extraction algorithm [5], [21]. The speech signal is represented, in general, in the frequency domain showing the temporal evolution of its spectrum. MFCC coding is based on the analysis by a Mel-scale filter bank to produce the MFCC cepstral parameters. In this algorithm, first the Discrete Fourier Transform (DFT) is used to calculate the frequency spectrum of the signal, and then the Discrete Cosine Transform (DCT) is used to further reduce redundant information in the speech signal. DFT and DCT can be used for any speech segment with a fixed time-frequency resolution. Equation (1) allowing the hertz to Mel is the most widely used [22] (it is a

common model for the relationship between frequencies in Mel scales and linear frequencies):

$$mel(f) = 2595 \times log_{10}(1 + \frac{f_{Linear\ frequency}}{700}) \quad (1)$$

For each tone with a real frequency f, measured in Hz, a subjective terrain is measured on a scale called the Mel scale. The pitch of a 1 kHz tone, 40 dB above the perceptual hearing threshold, is defined as 1000 mels. At the level of creating our voice database, we break down the database of teachers' names into two parts, the learning part and the test part. In our work the database consists of 1800 names pronounced by 24 people. Each person recorded 5 times the names of each teacher (each speaker pronounced 5 times each of the names of the teachers - see table 1). We used a total of 1125 names (15 teachers*75 times) for training and 675 names for testing. These numbers correspond to all the professors' names of the Electrical Engineering department of ENSAK school, so there were about 75 training data points and 45 test data points per professor.

Table 1. Number of examples for each class

NAMES (Classes)	Learning phase	Test phase
C1 : AILANE	75	45
C2 : AMHARECH	75	45
C3 : ATOUF	75	45
C4 : BENDAOUD	75	45
C5 : CHIKH	75	45
C6 : ELBARBRI	75	45
C7 : ERRACHID	75	45
C8 : EL JOURMI	75	45
C9 : HAMDOUN	75	45
C10 : KADIRI	75	45
C11 : KHAMLICH	75	45
C12 : LOKRITI	75	45
C13 : MAAIDER	75	45
C14 : MASSOUR	75	45
C15 : RHOFIR	75	45
Total	**1125**	**675**

After creating our voice database and encoding it in MATLAB, we tested some voice classification algorithms but we got a result that was not optimal. Then we tested on MATLAB the display of voice signals of the same message spoken by the same speaker under identical conditions, the display of the signals produces several different spectral shapes (see Fig.1).

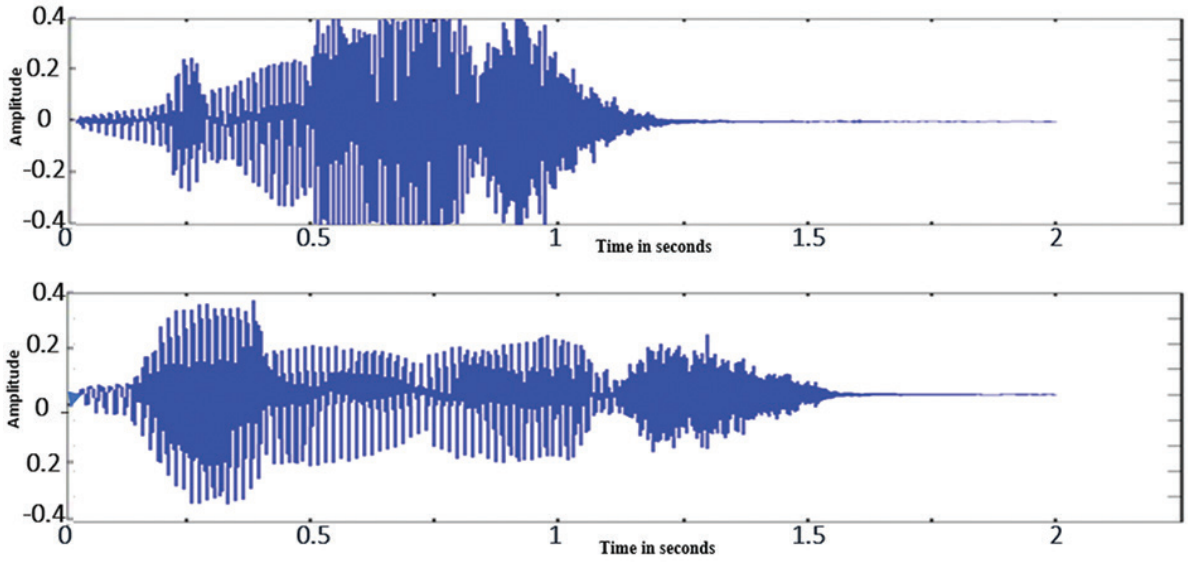


Fig.1. Name of Hamdoun pronounced by the same individual.

This variability is called intra-speaker [23]. The quality of the voice, the rate of speech, the degree of articulation are all factors at the basis of acoustic variations for a given signal. These variations lead to non-linear transformations over time of the speech signal. The non-linearity comes from the fact that the transformations affect the stable parts of the signal more than the phases of transitions [24]. To overcome this problem and that of computation time due to the size of the input vector we will use a preprocessing algorithm before using the recognition algorithms.

We move on to the step of storing the results (coded signal) in a \"text\" file to subsequently establish the previous steps of the extraction of speech characteristics by the MFCC algorithm [25]. Figure 2 shows the basic structure of audio signals and their extraction by the MFCC algorithm.

Individual Files N° 1 and **2** contain the audio files, their figures and their encodings. The contents of **Matrice_wav** folder are audio (matrix) files encoded by MATLAB the p' number of matrix elements is 16000

elements and the contents of **Vector_MFCC** folder are audio signal voiceprints. These are **p** input elements (p 1100 elements) of ANN and SVM.

After creating the fingerprints by MFCC, the vectors are divided into 2 parts one for training and another for testing. This method of extracting voice characteristics is an initial step and takes place before the achievement of voice recognition by the SVM and ANN algorithms. The main quality of the MFCC method is its biological plausibility since it uses a psycho-acoustic scale of frequencies similar to that of the inner ear [26-27].

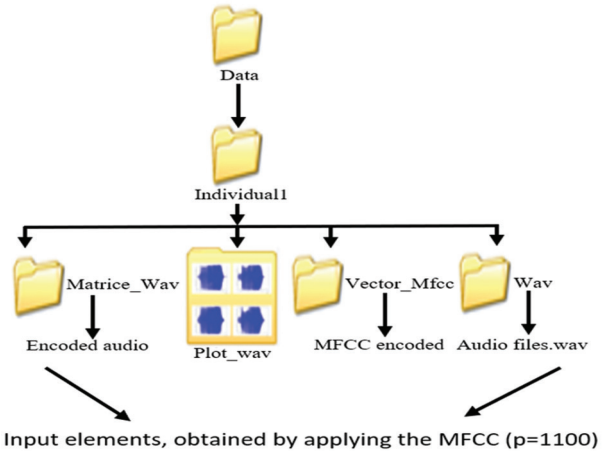


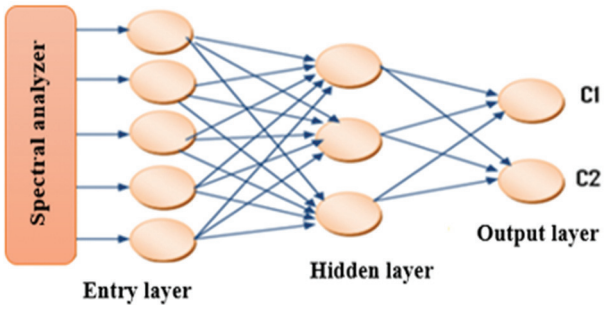
Fig. 2. Creation of a voice database

3.2. ARTIFICIAL NEURAL NETWORKS:

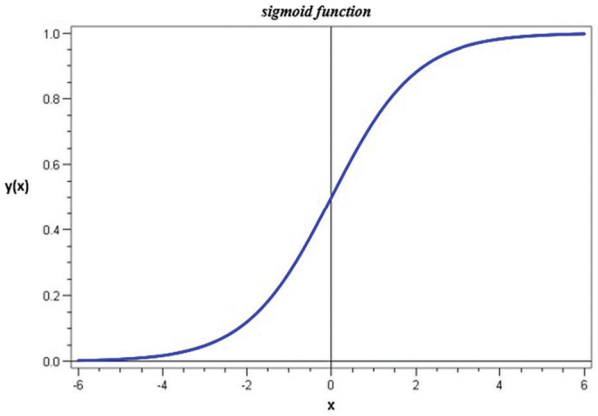
Automatic speech recognition is the process by which a computer issues an acoustic speech signal to text. It is carried out in this work by SVM and artificial neural networks (ANN) [28], in this part we have worked on the ANN. Artificial neural networks are mathematical and computational models [5] that mimic the functioning of the brain, including its ability to learn from examples and to generalize its knowledge [29]. There are different types of artificial neural network architectures, such as multilayer perceptron (MLP), recurrent networks, etc. [30]. These architectures require an example base to learn and an example base to test. The most widely used neural classifier is the MLP multilayer perceptron, which has also been widely analyzed and for which many learning algorithms have been developed [31].

A-Artificial neural networks MLP-type:

The creation of the MLP architecture depends on the parameters, such as the number of iterations, the number of hidden layers, the number of neurons in each layer, the training database, the test database and the learning rate. In the architecture of the multilayer Perceptron (See Fig.3 (a)), neurons in one layer are linked to all neurons in adjacent layers. The inputs of the functional unit of the first layer are calculated based on the inputs $\mathbf{X}_i$ and the weights of the links $\mathbf{W}_j$, the inputs of the functional unit of the second layer are the outputs of the first layer as well as their associated weights. The same principle holds for the output layer. The overall output of each MLP neuron is based on a sigmoid function which aims to keep the output in the interval [0,1] (See Fig.3 (b)).



a)



b)

Fig.3. a) Example of the MLP for isolated word recognition; b) Most significant interval of the sigmoid activation function.

Equations (2-4) represent the calculation of the outputs of each layer (example of two hidden layers). The synaptic weights are stored in the weight matrices denoted $\mathbf{W}_1$ (synaptic weights between the input vector $\mathbf{X}_i$ and the neurons of the 1st hidden layer) and $\mathbf{W}_2$ (synaptic weights between the 1st hidden layer and the outputs). The element (**i**, **j**) of a weight matrix represents the weight of the connection between neuron **j** of the downstream layer and neuron **i** of the upstream layer. The output of each neuron from each hidden layer is a sigmoid function. **F1** is the activation function associated with the first hidden layer, **F2** is the activation function associated with the second hidden layer (output layer in our architecture). In general, the activation functions are nonlinear and sigmoid in type (its main advantage is its derivability at all points).

The output layer:

$$S(z) = F2(ys(z)) = 1/(1 + e\text{^}(-y_s(z))) \quad (2)$$

Such as:

$$y_s(z) = \sum_{i=0}^{j} W_2(i,z) * F_1\,(y(i)) \quad (3)$$

So:

$$y(j) = \sum_{i=0}^{n} W_1(i,j) * X_i \quad (4)$$

Setting up a multilayer perceptron to solve a problem therefore involves determining the best weights applicable to each of the inter-neuronal connections. In this work, we have focused on automatic speech recognition. This determination is carried out through an MLP (multilayer perceptron) error back propagation algorithm.

B-Phases of MLP learning and testing

The multilayer perceptron architecture consists of an input layer which represents the object elements of the speech signal after extraction by the MFCC algorithm, of one or more hidden layers and an output layer representing the Classes (in our case the classes are the 15 names of the professors the department). After modifying these parameters and testing several MLP architectures, we obtained different results, but the best obtained results are presented in the following.

In this study, the number of neurons in the p 1100 input layer of the MLP corresponds to the number of characteristics of the input signal obtained by the application of the MFCC. The number of neurons in the output layer is fixed at 15 (the number of classes used to train the MLP).

To determine the number of hidden layers and the number of neurons to assign to each hidden layer, we have previously performed an experimental work. After the variation of the characteristics (e.g. change of neurons for a single hidden layer, increase of numbers of hidden layers, variation of iteration numbers and the database) we carried out the study with the aim of choosing the right values to obtain the right classification and recognition results. Figure 4 illustrates the learning steps that consist of calling a library (**hpp** folder) by the main program (src folder) as well as the MLP parameters (**arch_MLP** folder) and loading the database (step 3). We follow the same steps for the test but this time **step 3** is replaced by **step 4**.

Fig.4. Stages of learning and generalization

In our experiments, we first tested the MLP network with a single hidden layer. By varying the number of neurons in this layer, we found that the best results are obtained with a hidden layer of 7 neurons. In Fig.5 (A), we report the obtained results (global error) and express them in terms of learning and comprehension rate. The comprehension rate refers to the percentage of recognition of a word spoken by a speaker (in the testing phase) that does not already exist in the database

Then we worked out further experiments by adding another hidden layer. We fixed the number of neurons in the first hidden layer at 7 and in the second layer we varied the number of its neurons in order to find the most suitable architecture for our application. From the results shown in Fig.5 (B) we notice that the architecture using two hidden layers (7 in the first and 8 in the second) presents better results compared to other candidate architectures with two hidden layers. Despite the good results of this architecture, the MLP with a single hidden layer (containing 7 neurons) achieves better results compared to the MLP with two hidden layers.

For an architecture of three hidden layers, we followed the same steps as the second hidden layer. We set the number of neurons of the first hidden layer to 7, the number of neurons of the second to 8 and we varied the number of neurons of the third hidden layer, the results in Fig.5 (C) show that the MLP with a single hidden layer (containing 7 neurons) still offers the best performance.

In the architecture comprising a single hidden layer made up of 7 neurons, we varied the number of iterations depending on the overall error (see Fig.5 (D)). By analyzing this figure, we see that the increase in the number of iterations leads to a decrease in the overall error during the learning phases.

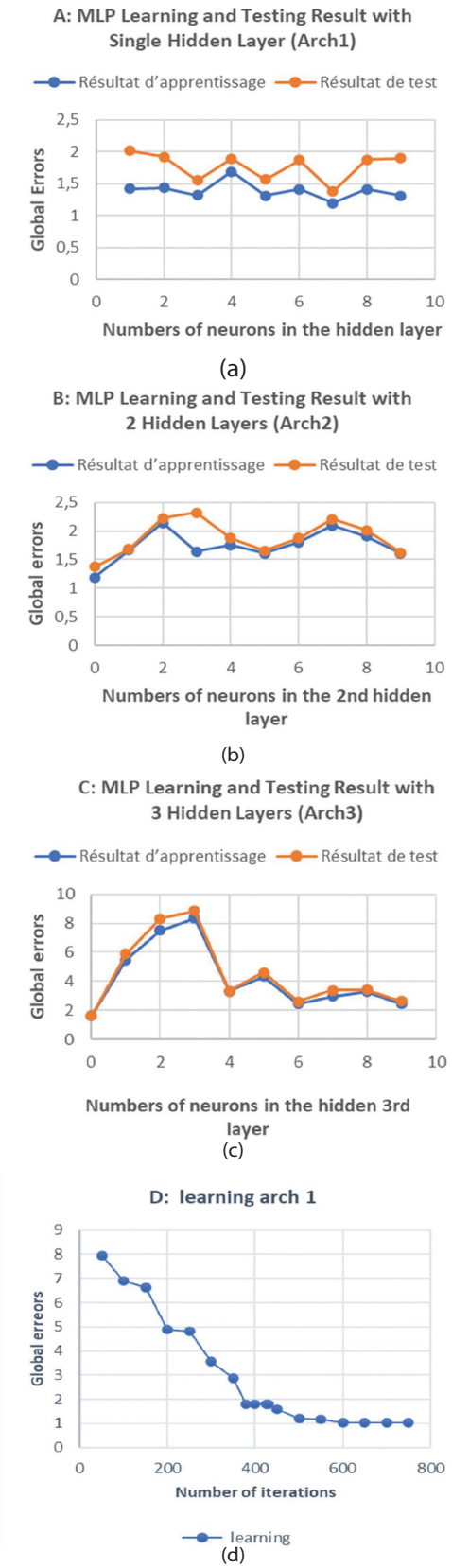


Fig. 5. a): Understanding rate and efficiency obtained with our MLP by varying the number of neurons using Single hidden layer (Arch1). **b)** Comprehension rate and efficiency obtained with MLPs with two hidden layers (Arch2). **c)** Comprehension rate and efficiency obtained with MLPs with three hidden layers (Arch3). **d)** Global error change depending on the number of iterations of Arch1.

Table 2 summarizes the best results of the 3 architectures discussed previously, with Tmax representing the maximum number of iterations. Testing of MLP with two and three hidden layers did not perform better results than those obtained using a single hidden layer. The architecture we have proposed for speech recognition has proven its effectiveness in our application and the result is quite significant. This confirmed the interest of the approach adopted in this study.

Table 2. Results of the neuronal classification of the three architectures 1, 2 and 3.

	Hidden layer 1	Hidden layer 2	Hidden layer 3	Number of iterations	Minimum Error %	Tmax
Arch 1	7 neurons	---	---	600	1.03851	3407
Arch 2	7 neurons	9 neurons	---	620	1.592432	3424
Arch 3	7 neurons	9 neurons	6 neurons	570	2.42865	3729

In this study, we have obtained several satisfactory experimental results that can be use in other similar applications. Among these values, we choose:

- One single hidden layer.
- 7 neurons in the hidden layer.

In comparison to the best result of our architecture after implementation with traditional digital implementations of artificial neural networks, our implementations simplify the complexity of the calculation and the economy of digital resources with a reduced footprint.

3.3. MULTI-CLASS SVM FOR AUTOMATIC RECOGNITION OF 15 NAMES.

SVMs (Support Vector Machines) are new techniques of supervised statistical learning that allow to create a decision surface between two classes defined in the same space (binary and statistical classifiers) [32]. One needs to provide a training dataset to build the classifier.

Several studies have been able to show the effectiveness of these techniques mainly in image processing [33]. The essential idea of SVM consists in projecting the input space's data (belonging to two different classes) non-linearly separable in a space of greater dimension called the characteristic space so that the data becomes linearly separable (See Fig.6). In this space, the optimal hyperplane construction technique is used to calculate the ranking function separating the two classes.

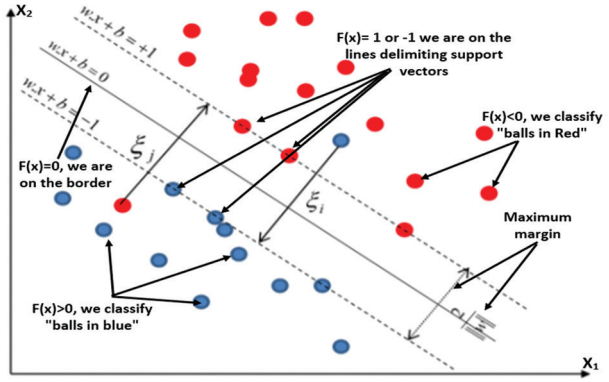


Fig. 6. Illustration space of characteristics of SVMs

The conventional SVM-based pattern recognition system can be schematized, as shown in Fig.7. SVMs require input vectors of fixed lengths that represent a whole word. They therefore propose a method to overcome this problem. After extracting the parameters of the speech signal by the MFCC method, these parameters are used as data input for the classification component (SVM), which will look for a separating hyperplane that separates the examples in the learning phase and makes a classification decision in the identification phase. The approach we have adopted is based on removing MFCC vectors at times when MFCCs change the least until there are only MFCC vectors remaining in the feature set, the algorithm in [32] represents the reduction method.

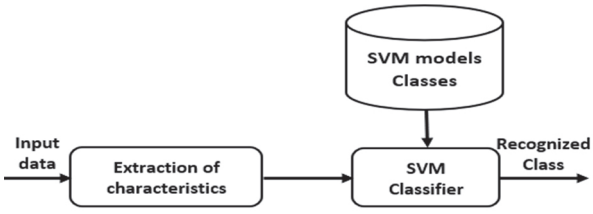


Fig. 7. Conventional SVM-based pattern recognition system [34].

Then, MFCC delete frames for which the difference between two successive frames is minimum. In the SVM module, there are two phases like the method used in the MLP-type ANN one for learning and the other for testing. In this part, we will use the two main methods of multi-class binary classification (Multi-class SVM) as a pattern recognition technique, one-against-one and one-against-all, in order to increase the reliability of the resulting system. One-against-one (1vs1), also called 'pairwise', is due to Kner et al. [35]. One-against-all (1 vs all) is the easiest and oldest method. According to the formulation of Vapnik [36], it consists in determining for each class k a hyperplane Hk (wk, bk) separating it from all the other classes. Figure.8 represents a case of separation of 3 classes.

In the next part we have combined classifiers of the same multi-class SVM type (SVM one against all and SVM one against one).

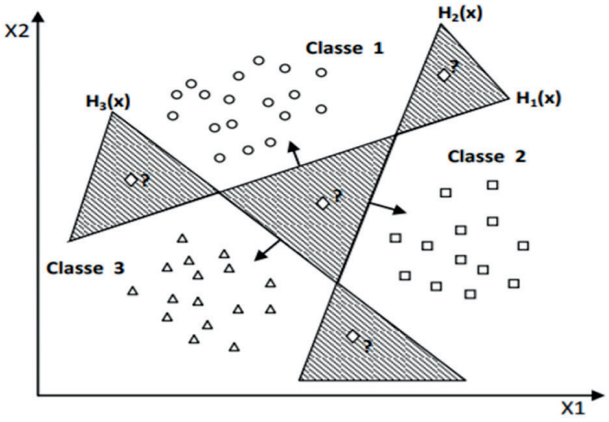


Fig. 8. One-against-rest approach with areas of indecision.

3.3.1. Summary of the SVM algorithm used: SVM learning and testing phases:

We used the same database which is used in ANN. This represents approximately 75 training points and 45 test points for each name (see table 1). All the speakers are adults (women and men). The signal is sampled at 8kHz, encoded on 32 bits. The learning and testing of SVMs were carried out using the LIBSVM software (Install and implement in MATLAB) which allows the classification of the algorithms that are described in [37], using MATLAB on a computer with a 2.8 GHz Intel i7-7700HQ processor with 16 GB of RAM. The LIBSVM library is developed with the aim of simplifying the use of SVMs as a tool. In this work we are using the libsvm-3.24 version in MATLAB. It was released on September 11th, 2019. The results of the training are the following parameters (Alpha, SVs, Bias b, nSV) necessary for the construction of the SVM classifier. In this work we combined classifiers of the same multi-class SVM type in parallel and then we tested their learning capacity. We used the same training base as well as combining the Principal Component Analysis (PCA) and Linear Discriminant Analysis (LDA) in the same chain with the alignment algorithm. Tables 3 and 4 give the confusion matrices for the two classifiers.

3.3.2. SVM learning and testing phases:

A-chain based on one-on-one SVM with the fusion between ADL and ACP:

If we use the fusion of LDA and PCA, the retained values are (C=10 and γ=0.0028) which made it possible to obtain an almost zero error rate on the learning basis (test by the corpus of learning), and an error rate of 1,813% on the test basis. The PCA algorithm reduces the dimensionality of the space by eliminating the lowest eigenvalues, and the ADL aims to maximize interclass variations while minimizing intra-class variations. The confusion matrix for the next string: Pre-emphasis → MFCC → Reduction by PCA and LDA (Size vector adapted to SVM classifiers) → SVM one against one is shown in table 3:

Table 3. Confusion Matrix for SVM (One to One)

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
C1	98.88	0.90	0	0	0.16	0	0	0	0	0	0	0.05	0	0	0
C2	0.04	98.35	0	0.05	0	0.28	0.2	0.01	0.22	0.1	0	0.6	0	0.15	0
C3	0	0	98.23	0	0	0.34	1.33	0	0	0	0	0	0.1	0	0
C4	1.2	0	0	97.89	0	0	0	0.2	0.45	0	0	0	0	0	0.25
C5	0.88	0	0	0.44	96.9	0	0	0.88	0	0	0	0.8	0.1	0	0
C6	0	0	0.33	0	0	99.56	0	0	0	0	0	0	0.11	0	0
C7	0.05	0	0	0	0	1.70	98.02	0.06	0	0	0	0	0	0	0.14
C8	1.33	0.32	0	0	0	0.12	0	97.83	0	0	0	0	0	0.40	0
C9	0	0	0	0	1.77	0	0.44	0	96.90	0	0	0	0.2	0.4	0.28
C10	0	0	0.46	0	0	0	0	0	0	97.79	0.42	0	0	0.44	0.88
C11	0	1.11	0	0.10	0	0	0	0	1.1	0	97.36	0	0	0	0.33
C12	0.88	0	0	0	0	0	0	0	0	0.88	0.88	96.46	0	0.88	0
C13	0.44	0	1.10	0	0	0	0	0	0.44	0	0.33	0	96.81	0	0.88
C14	0.21	0	0	0.10	1	0	0	0	0	0	0	0	0	98.48	0.21
C15	0.33	0	0.33	0.22	0	0	0	0	0.44	0	0	0	0	0.33	98.35

B- One-against-all SVM-based chain with the merger between LDA and PCA

If we use the one-against-all SVM classifier instead of the one-against-one SVM classifier with the serial combination of PCA and LDA in the recognition chain, we get an almost zero error rate on the learning basis (test by the learning corpus) and an error rate of 5.38% on the test basis. The recognition rate in this case shows that the classification using the one-on-one SVM algorithm is more efficient than the classification using the one-on-all SVM algorithm. The confusion matrix for the following chain: Pre-emphasis → MFCC → Reduction by PCA and LDA (Size vector adapted to SVM classifiers) → SVM one against all is shown in Table 4:

Table 4. Confusion matrix for SVM (one vs. all)

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
C1	95.42	1.12	0.2	0	2.2	0	1.05	0	0	0	0	0	0	0	0
C2	0	96.02	0	0	0	0.44	1.33	0.88	0.00	0	0	1.33	0	0	0
C3	0	0	97.35	0	0	0.24	0.64	0	0	0	0	0	0.88	0	0.88
C4	0	0	0	96.46	0	0	0	0	0.88	0	0	0	2.21	0	0.44
C5	0.44	0	0	0.88	94.2	0	0	1.33	0	0	0	0.88	1.77	0.05	0.44
C6	0	0	2.21	0	0	93.36	0	0	0	0	0	3.10	1.33	0	0
C7	0.88	3.10	0	0	0	0	93.81	0.44	0	0	0	0	0.44	0	1.33
C8	0.44	0	2.10	1	0.22	0	0	93.81	0.22	0	1.33	0	0	0	0.88
C9	0.44	0	0	0	1.33	0	0	0	96.46	0	0	0	0.44	1.33	0
C10	0.88	1	0	0	0	0	0	1.8	0	92.01	0	0	0	0	2.10
C11	0	0	0.33	0.40	0	0	0	0	0.11	0	96.70	0.11	00.13	0.55	1.66
C12	0.3	1.1	0	1.6	0.7	0.41	0	0.2	1.1	0	0	93.36	0	0	1.03
C13	1.77	0.88	0	1.33	0	0.88	0	0.44	0	0.44	0	0	94.25	0	0
C14	3.62	0.44	0.44	1.54	0.88	0	0.44	0	0	0.44	0	0	0.77	90.97	0.44
C15	0.88	0	2.20	0.22	0	0	0	0.1	1.33	0	0	0	0.44	0.33	95.13

Depending on the table and the learning phase, the results show a lower average recognition rate than the previous chain but the classification rate obtained by this chain is also acceptable.

4. RESULTS AND DISCUSSIONS

Figure 9 shows the performance of the three architectures (Arch1, Arch2 and Arch3) of the MLP (this is a summary of Fig.5 (a), (b) and (c) and (d)) in terms of overall errors, number of hidden layers, number of neurons in each layer and number of iterations (see Table 2). The study is based on the application of voice recognition of the names of 15 people (15 classes) in our department.

For the multi-class classification, two approaches have been adopted: the first consists of a one-to-all classification, the second approach consists of a 1-to-1 classification. Figure 10 gives a comparison of the error

rates between the two SVM and MLP classifiers, during the learning and testing phase (We have based on Tables 2, 3 and 4 for the three classifiers MLP-ANN (a single hidden layer consisting of 7 neurons), SVM (one vs all) and SVM (one vs one)). By simply comparing our results (SVM one against all / SVM one against one) we notice that the recognition by a classifier using the one against one strategy with the merger between LDA and PCA is much more satisfactory compared to the classifier using the one against all strategy.

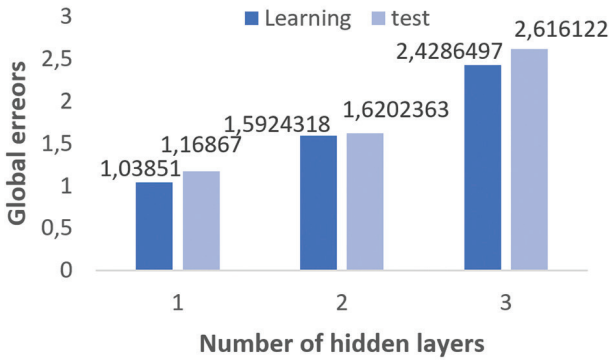


Fig. 9. Comparison between the three best architectures (Arch1, Arch2 and Arch3)

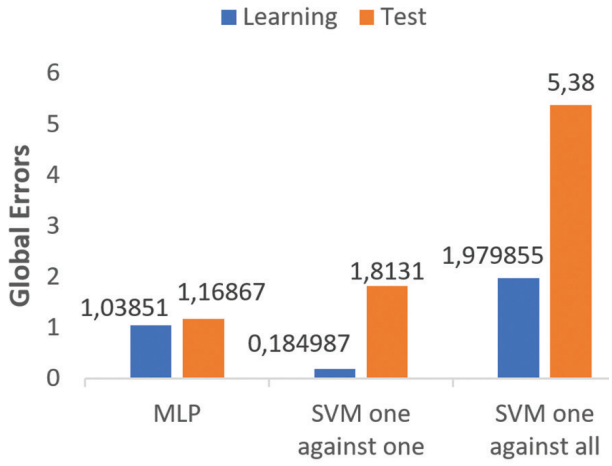


Fig. 10. Comparison between the best results of the three classifiers (Global error rate)

We notice that the classification rate is high even with few training samples, which shows its power of generalization. Since SVM is used to solve support vectors using quadratic programming, that will involve the computation of the order matrix. When the number of samples is large, storing and computing the array will consume a large amount of machine memory and runtime. We can say that there is not a great deal of difference between SVM one against one and the MLP-ANN. But the classification method based on MLP-ANN is the fastest and its size also leads to a allocation of reduced space in the hardware during implementation.

Among the objectives in our application, we cite the development and implementation of the techniques described previously in an FPGA card based on the embedded NIOSII processor. This technique is presented in the next section.

5. HARDWARE IMPLEMENTATION OF MFCC AND MLP-ANN ALGORITHMS:

In this work we have created a voice recognition system based on SVM and artificial neural networks of MLP type. In this part we will present the hardware architecture of the proposed MLP which is based on an input vector (voice signal after extraction by MFCC) and an output vector representing the 15 classes.

5.1. MFCC HARDWARE IMPLEMENTATION:

This part deals with the hardware implementation in the FPGA version DE2-70 board, produced by the company Altera [38] of the MFCC algorithm. According to Fig.11, the system receives a signal of an analog nature which comes from the microphone and sends it to the analog-to-digital converter ADC integrated in the codec circuit [39] to sample our signal at the frequency of 8Khz producing an output of digital samples. Each sample is coded on 32 signed bits. The output of the converter is linked with 2 registers (left register and right register) the size of each is 16 bits. The Hamming windowing and the discrete fourrier transform DFT are applied to the output of these registers, which will be responsible for calculating the DFT of this vocal piece. The windowing and DFT modules are included in the on-board NIOS II processor which reads the outputs of the DFT, and checks whether the vocal piece corresponds to silence or to a speech signal [40]. If it detects a speech signal, the NIOS II processor performs the various calculations [41], [42]. such as normalization, feature extraction, and fingerprint storage in SDRAM memory.

The block diagram below represents the entire system:

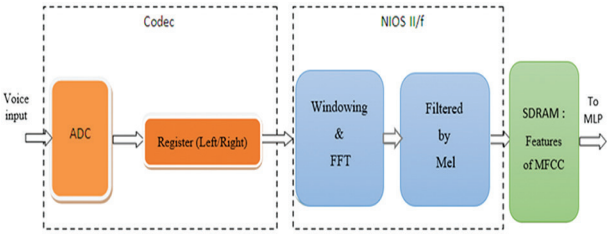
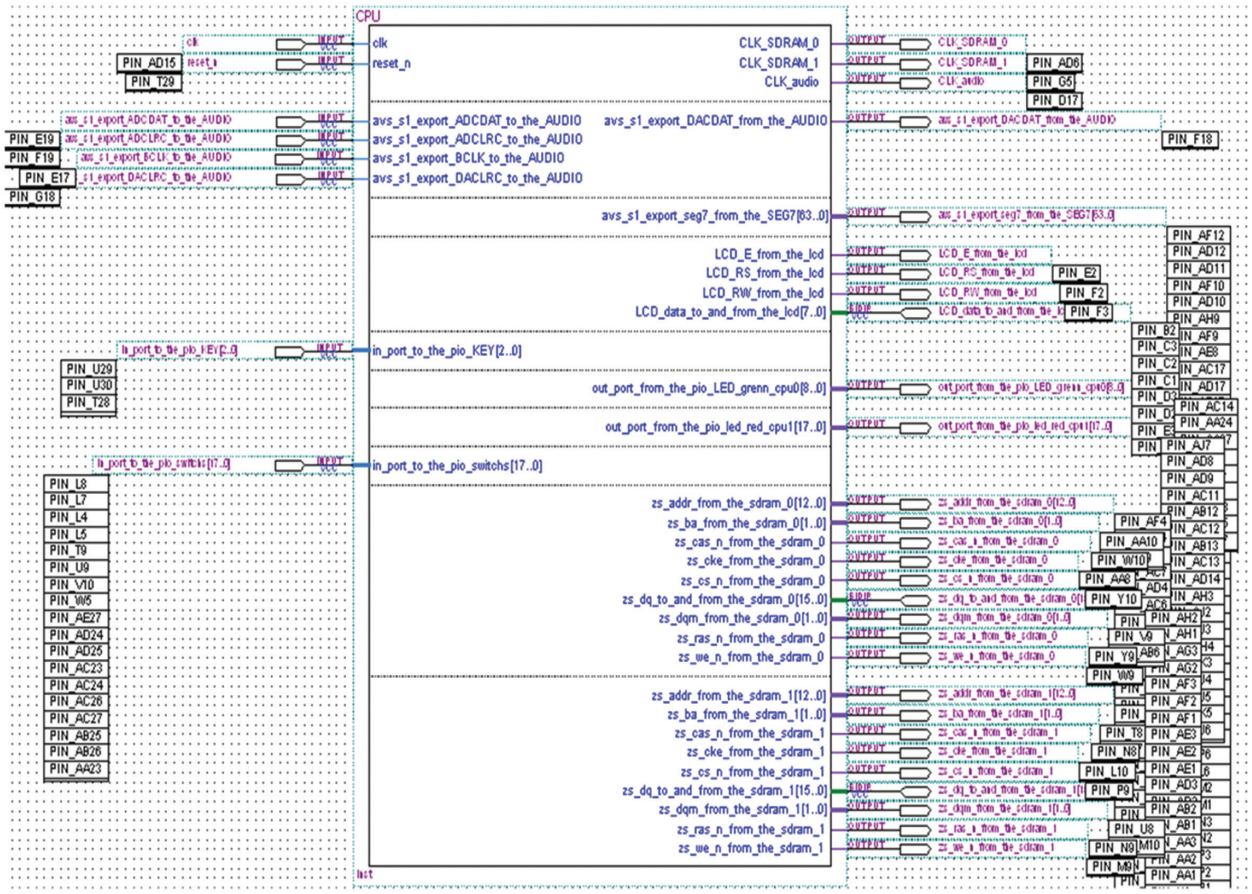


Fig.11. Hardware voice signal extraction

Figure 12 (a) shows the complete design of our NIOSII and Fig.12 (b) shows the compilation result of this Hardware processor by QUARTUS software [38], [43] and [44].

The implementation of the hardware part of the various peripherals constituting our system leaves enough space on the programmable FPGA component version EP2C70F896C6 for the addition of other peripherals or the hardware integration of speech processing algorithms.



a)

Flow Status	Successful - Sat Jul 13 20:00:55 2013
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	mupross
Top-level Entity Name	mupross
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	No
Total logic elements	6,607 / 68,416 (10 %)
Total combinational functions	5,230 / 68,416 (8 %)
Dedicated logic registers	4,151 / 68,416 (6 %)
Total registers	4289
Total pins	249 / 622 (40 %)
Total virtual pins	0
Total memory bits	472,128 / 1,152,000 (41 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	1 / 4 (25 %)

b)

Fig.12. (a): Hardware processor created in the FPGA circuit. (b): Hardware space reserved by our processor.

5.2. MLP HARDWARE IMPLEMENTATION:

In this study we obtained many satisfactory values, that we can use in applications similar to our application. Among these values, we choose:

- The number of neurons in the MLP input layer are p = 1100.
- A single hidden layer.
- 7 neurons in the hidden layer.
- The number of neurons in the output layer is fixed at c = 15.

As we can see in equations (2) and (3), the basic calculations of a single neuron are the multiplication of the outputs of the connected neurons by their associated weights, and the sum of these multiplied terms. Figure 13 describes the basic structure of the functional unit used for the serial hardware implementation [45] that performs these calculations. It includes a multiplier for multiplying the elements of the input vector with their corresponding weights. A sign extender is placed immediately after the multiplier. The input of the accumulative adder is connected to the output of the expansion unit.

The output of the accumulator is linked to the input of the adder. This functional unit has been implemented in the FPGA board.

For the implementation of MLP, we established the data encoding namely, inputs, outputs, weights, activation function, etc. therefore, it is necessary to limit the number of different variables:

- Two among MLP inputs and outputs of the activation functions of different neurons must have the same range to be able to easily manage multiple layers of processing. In this context, we have chosen 32-bit encoding.
- Weight of connections of MLP neurons (32-bit coding).

The primary storage strategy is to use SDRAM memory modules such that inputs, outputs, and connection

weights are stored in these modules. In what follows, we will describe in detail the software implementation of MLP (parallel). This type of implementation is given at two different levels of abstraction [45].

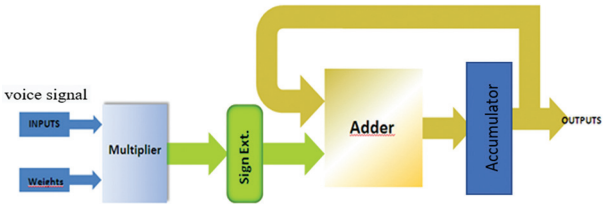


Fig.13. Hardware structure of the functional unit

To program the HW processor (see figure 12 (a)), figure 14 shows the structure of our software directory for the MFCC and MLP implementation (see HW processor Fig.11 and 13) based on the NIOSII multiprocessor.

The distribution of our multiprocessor software system for speech processing:

Software_khamlich file is containing our multiprocessor system NIOSII software This file is subdivided into the following subfolders.

- **Khamlich_CPU1** folder: main folder containing the folders and files of our program for audio signal recording, status display etc (same folder for a single processor).
- **Khamlich_CPU2** folder: main folder of the MFCC algorithm to extract the audio signal before recording.
- **Khamlich_CPU1_bsp** and **khamlich_CPU2_bsp** folders: the libraries of useful functions to define the process.

The connection between the hardware and software parts is done through the system.h file which contains the address of the registers of our IP block. The data transfer between the coprocessor and the memory is done through the Avalon bus. After the compilation of our processor HW (Fig.12 (a)) and SW (Fig.14) we created a file for the operating simulation (recording and playback) of the voice signal. The program of each processor must be located in its own memory area and to avoid the conflict between the program memory areas of each processor, it is better to put the program of each processor in a different memory.

Fig.14. Program structure of our NIOSII multiprocessor

6. IMPLEMENTATION RESULTS

Figure 15 illustrates the results of our processor implementation and speech processing algorithms. The results of this application after the implementation of the algorithms can be characterized by the following parameters number of ALUTs, number of onboard SDRAM memory blocks, maximum clock frequency, etc. To solve the real-time speech recognition problem, our application requires NIOSII / fast processors. After the implementations of these processors and the MFCC and MLP algorithms, the maximum recorded execution time obtained in our result, has undergone approximately 45% of reduction.

Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	No
Total logic elements	6,339 / 68,416 (9 %)
Total combinational functions	5,261 / 68,416 (8 %)
Dedicated logic registers	3,782 / 68,416 (6 %)
Total registers	3920
Total pins	534 / 622 (86 %)
Total virtual pins	0
Total memory bits	147,392 / 1,152,000 (13 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	1 / 4 (25 %)

Fig. 15. Size of our hardware architecture

So, the FPGA hardware / software design method described in this article offers many advantages over microcontroller-based solutions, including tailoring the hardware configuration to the needs of the application, protecting against obsolescence and for real-time processing, the integration of custom hardware accelerators. With the NIOSII processor and the Cyclone2 FPGA, embedded system designers can configure a processor-based system to perfectly suit their needs, which is impossible to achieve with frozen and peripheral-limited sets of a standard microcontroller. Our Nios II processor is credited with unprecedented flexibility for cost-sensitive, real-time processing, and security-critical systems [42].

7. CONCLUSION

In this work we used the multi-speaker mode and we examined the applications of wide margin separators (SVMs) and MLP for the classification of names of professors in ENSAK school. SVM algorithms with the one-on-one approach and MLP-ANN are the most suitable because of their efficiency. They outperform SVM (one against all) in both classification rate and execution time. After testing several classification architectures, we chose the MFCC coding method for the parameterization of the acoustic signal and the MLP-ANN method for the recognition of isolated words. The two multi-class classification strategies: one against one, and one against all, were used in order to choose the best classifiers. The MFCC is used for extracting voice data and to increase the reliability of the resulting system.

Following several changes in the internal FPGA circuit architecture, we have chosen the best hardware processors that are suitable for our speech processing application. The cores of these NIOSII programmable processors and the elements for mapping the MFCC and MLP architectures are implemented in parallel in the FPGA circuit. These processors were used for the purpose of testing our application and choosing the best one. We have created two on-board processors; the first processor is used by MLP-ANN for classification and the second is used for future voice signal extraction by MFCC and, their implementation of MLP. We used only the adjusted synaptic weights, numbers of hidden layers, numbers of neurons in each layer and numbers of classes. This gives us an advantage of MLP. We don't need a memory to store a base of the signals for comparison with the voice input signal. So, our implementation makes it possible to simplify the complexity of the calculation and to save digital resources, figure 12 (b) illustrates the size reserved in the FPGA circuit by our NIOSII.

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Expiry Prediction and Reducing Food Wastage using IoT and ML

Original Scientific Paper

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Abstract *– This paper details development of a low-cost, small-size, and portable electronic nose (E-nose) for the prediction of the expiry date of food products. The Sensor array is composed of commercially available metal oxide semiconductors sensors like MQ2 sensor, temperature sensor, and humidity sensor, which were interfaced with the help of ESP8266 and Arduino Uno for data acquisition, storage, and analysis of the dataset consisting of the odor from the fruit at different ripening stages. The developed system is used to analyze gas sensor values from various fruits like bananas and tomatoes. Responding signals of the e-nose were extracted and analyzed. Based on the obtained data we applied a few machine learning algorithms to predict if a banana is stale or not. Logistic regression, Decision Tree Classifier, Support Vector Classifier (SVC) & K-Nearest Neighbours (KNN) classifiers were the binary classification algorithms used to determine whether the fruit became stale or not. We achieved an accuracy of 97.05%. These results prove that e-nose has the potential of assessing fruits and vegetable freshness and predict their expiry date, thus reducing food wastage.*

Keywords *– electronic nose (E-nose), MQ2 sensor, food expiry prediction, food wastage, machine learning*

1. INTRODUCTION

Today, many food products come with labels – "Best By" or "Use By" stamped on the packaging. But what do they mean? 37% of users reported that they discard food each time it's past the expiry date – however the date only denotes peak quality determined by the manufacturer. The manufacturer tests the food in a controlled environment. However, during transportation from Farm-to-Fridge, it undergoes mishandling and temperature fluctuations. Thus, the expiry date mentioned on the packaging is not accurate anymore and this ambiguity leads to food wastage in large quantities around the world, daily [6]. Farmers tend to keep the food products in the warehouses for a long period before sending them to the market, causing food wastage in large quantities since one spoilt batch usually spoils the entire batch. The farmers incur heavy losses which in turn leads to increased prices thus, adversely affecting the economy. This is one of the major reasons for the fluctuating prices of fruits and vegetables.

Earlier research has been done on the detection of different ripening stages of bananas using Computer Vision [9]. For example, a camera system has been proposed to observe the peel color on the surface of the fruit as an additional feature. The dual E-nose/camera system depicts the Fisher class separability measure. It displays a perfect classification of the four maturity stages of a banana: Unripe, half-ripe, fully ripe, and overripe [11]. In another method, the Raspberry Pi 3 Model B was used to collect and display the data from a sampling and sensor chamber. The sensor chamber consisted of 7 types of MQ sensors that were detecting the gas being released from tomato-based Filipino cuisine [2].

But these methods will be computationally expensive and memory exhaustive for storing the data and applying machine learning algorithms. Instead, we have approached the problem using temperature, humidity, and gas sensors that detect the emission of combustible gases from the food products (e.g., Banana and Tomato). Using this method, we obtained numeric values

to build the dataset ourselves. The MQ2 gas sensor was linked to the Blink IoT application using the ESP8266 module. The banana is placed in the sample chamber and the sensors capture data every 30 seconds. The values are automatically logged into a CSV file. We noticed an incremental graph of the gas concentration over a 5 days course. Based on the obtained data, we applied machine learning algorithms: Logistic regression, Decision Tree Classifier, Support Vector Classifier (SVC) & K-Nearest Neighbours (KNN) classifier to predict if a banana is stale or not. We achieved an accuracy of 95.9% with the Support Vector Classifier. The same procedure is being applied to other fruits and vegetables too.

The system can be used in warehouses for food storage by manufacturers, the food processing industry, and supermarkets to monitor food quality in real-time and help the consumer gain complete transparency about the food they consume [1]. If people know exactly when their food is going to spoil, they can consume, donate, or convert it to compost. This way, food wastage reduces tremendously and the traditional methods of discarding food (which leads to increased Co2) can be avoided. The Agro-benefits can be seen where a farmer can predict and plan the distribution of his produce. As soon as one batch of the product is ready and ripe, the farmer will be notified, and he can quickly sell his product. The system will also notify him if one batch becomes overripe so that the other products can be saved. This will also minimize fluctuations in the global food economy. Overall, the project holds multiple benefits in addition to the above that can also be explored.

Fruits like bananas are usually stored together in a warehouse, a ripening wave is initiated due to the ethylene gas being emitted from the first banana [10]. This process expedites the ripening of other bananas as well, thus leading to the over-ripening of food products sooner than expected. Thus, constant monitoring is required to reduce food wastage.

2. LITERATURE SURVEY

The solution to cur pollution by monitoring air quality is presented in the form of a prototype that uses semiconductor gas sensors like MQ4 and MQ7. MQ7 can be used to detect carbon monoxide concentration in the range of 20 to 2000 ppm. The tin dioxide of the sensor reacts with carbon monoxide which results in the reduction of the sensor resistance. This reduction is an indication of an increase in the output voltage, which can now be measured. MQ4 sensor is used to detect natural gases like methane in the concentration range of 200 to 10,000 ppm. An LM35 sensor is also being used to obtain the output directly in the centigrade scale. Further, air quality was estimated based on Air Quality Index (AQI) guidelines set by the Central Pollution Board (CPCB). However, the prototype needs to be implemented on a larger scale to make an impact in reducing pollution. Additional ways to curb pollution must be suggested. In future systems, alerts using SMS or E-mail can be provided [3].

In this paper, the development of a small-size, low-cost portable e-nose has been discussed. Metal oxide semiconductors by Figaro have been used for the sensor array. PIC18F4520 is used in the Embedded E-nose and RS 232 is used to interface it to the PC for the acquisition, storage, and analysis of the data set consisting of odor signals from oranges and onions. The PIC18f4520 is used to control the sensor heaters and record the sensor response. It is interfaced to the sensor array consisting of 10 metal oxide semiconductor (MOS) sensors like TGS-813 and TGS-816 as well as temperature and humidity sensors like LM-35 and SY-HS-220 respectively using programmable gain amplifiers (PGA). Four quads op-amp LM 324 IC is used as a unity gain amplifier as the signal conditioning unit to avoid loading. It was observed that the responses to food like onion and rotten onion were different. Thus, showing that this Embedded E-nose has shown promising results. However, pattern recognition algorithms still need to be developed and applied to identify the odor and freshness of food [4].

This project proposed a metal oxide semiconductor-based cost-effective E-nose that was able to differentiate between the different ripening stages of a banana. It was able to identify the difference between the aroma fingerprint of bananas and achieved an accuracy of 98.66% accuracy using Support Vector Machines (SVM). The experimental setup included four stages: (1) a sampling system, (2) a gas sensor array, (3) a data acquisition system, and (4) pattern recognition algorithms. 15 bananas varying in color, size, weight was placed inside the sampling chamber where the gas level (ethylene) and temperature were being controlled and monitored. The cycloid gas chamber consisted of 6 MOS sensors (MQ-3, MQ-5, MQ-9, MQ-131, MQ-135, MQ-136), and using the data acquisition card, the gas sensor readings were stored in the computer and used for analysis to extract vital information. Principal component analysis (PCA), linear discriminant analysis (LDA), SIMCA, and SVM were the methods used for data analysis. SVM separates the classes using a hyperplane, which maximizes a quantity called margin and can be used for non-linear data as well. Thus, a low-cost MOS-based e-nose was designed to identify and differentiate between the different ripening stages of an e-nose. However, further work to develop additional sensors and an estimate about the right number of sensors need to be determined [7].

The review discusses the application of E-nose and E-tongue in determining properties that are related to food quality. Various sensors used in E-nose and tongue are compared based on the working principle, application, and limitation. Gas sensors like conducting polymers (CP), metal-oxide-semiconductor (MOS), quartz crystal microbalance (QCM), and surface acoustic wave (SAW) sensors can be used to develop an E-nose. These

sensors then react with the target chemicals and cause irreversible changes in electrical properties like conductivity. MOS sensors are sensitive to hydrogen and unsaturated hydrocarbons and used metal oxide semiconductors like iron or zinc oxide. However, these sensors consume a high amount of energy as they have constraints related to working temperature conditions (between 150 to 400 °C). CP sensors operate without external heating and hence consume less power than MOS sensors. However, these are sensitive to humidity and temperature and hence, it becomes necessary to maintain the optimum conditions at all times.

The properties of food samples can be recognized using machine learning classifiers and algorithms like PCA and SVM. In some cases, it has been combined with other classifiers to determine food quality. The decision tree used ID3 as a training algorithm. It builds the decision tree using the top-to-bottom and greedy approach. Hence, decision trees and RF can also be used to determine certain aspects related to food quality. Gas sensors are in general, extremely sensitive to temperature and humidity and sample preparation and sampling both depend on these factors. Even the sample size has to be considerably large to achieve a high level of accuracy. E-nose also consumes a high level of energy which thus, hampers their ability. Only time-invariant information could be detected as ANN and PCA were both developed for static features. Hence, an E-nose, smaller in size, unaffected by external environmental features, consumes less energy and still gives a high level of accuracy, needed to be developed. In addition to this, E-nose had to be made more user-friendly [13].

In this project, an e-nose (PEN2, Airsense Analytics, GmBH, Germany) which consists of an auto-sampling apparatus, a sensor array, and a pattern recognizer software was used to detect the freshness of pork. The sensor array is made of ten MOS sensors lik3 W1C, W6S, and W3C. Factors like the mass of the pork samples, storage time, and headspace-generation time were used in the sampling procedure to determine the optimum experimental conditions. Linear Discriminant Analysis (LDA) and Back Propagation Neural Network (BPNN) were used to classify the pork samples based on storage times (ST) and showed an accuracy of 97.14%. Multiple Linear Regression was used to predict the sensory scores. The correlation coefficients (R2 = 0.9848) between the sensory scores and e-nose signal were high, thus proving that it can effectively assess pork freshness. The result showed that sensory scores of odor and viscosity reduced as storage time increased, especially after the third day. Thus, the algorithms applied were able to classify the pork samples during the storage period, thus predicting the storage time and sensory scores. They were well discriminated by LDA, classified correctly by BPNN and the quality index was provided by MLR. However, the PEN2 e-nose is comparatively expensive and not easily available. Also, additional Machine Learning algorithms need to be developed to increase accuracy and range [5].

In this paper, Electronic noses are being developed for the automated identification of volatile chemicals. They have described and developed a basic prototype of an Electronic Nose and discussed its' applications in the field of medicine, food, and the environment. Electronic Nose consists of a sensor array and Artificial Neural Networks (ANN). Each chemical vapor makes a particular signature/pattern when detected by a sensor. Introducing different chemical vapors will create a database of those signatures. ANN is then used to analyze the complex database and identify the chemical vapor. A prototype consisting of nine tin-oxide vapor sensors along with temperature and humidity sensors was built. The ANN used for this prototype was a multilayer feed-forward network trained with the backpropagation algorithm and the fuzzy ARTmap algorithm. This prototype was tested on five chemicals: acetone, ammonia, isopropanol, lighter fluid, and vinegar. The two networks were trained using randomly selected training patterns and an accuracy ranging from 89.7% to 98.2% was achieved. In the medical field, an electronic nose detects possible problems by analyzing odors from the human body. Using this can also reduce the amount of analytical chemistry used in food production and its applications are in assessing food quality, checking rancidity of mayonnaise, and grading of whiskey. However, it still needs to compare the prototype with the conventional systems as well as develop a field system. Also, additional neural networks should be applied to ensure the highest level of accuracy [14].

The ripeness of postharvest kiwifruit was predicted using an E-nose with 10 MOS sensors. Three different feature extraction methods like max/min values, difference values, and 70th values were used to discriminate the fruit at different stages. In addition to this, Partial least squares regression (PLSR), SVM, and random forest (RF) were used to predict overall ripeness, soluble solids content (SSC), and firmness. 160 kiwifruits were subdivided into groups of 20 each and stored in an incubator (20 °C and 70% relative humidity). PEN3 E-nose system was used to detect the gas from the samples. The E-nose was preheated to reach working temperature and sensor 2 (W5S) gave the most significant response. Further, SSC and firmness were used to determine the sweetness and hardness of kiwifruit. The three features were used along with LDA to classify the different ripening stages. RF algorithm showed the best performance with overall ripeness (training: R2 = 0.9928; testing: R 2 = 0.9928), SSC (training: R2 = 0.9749; testing: R2 = 0.9143) and firmness (training: R2 = 0.9814; testing: R2 = 0.9290). Thus, this study successfully predicted the ripeness of postharvest kiwifruit using a MOS E-nose using different feature extraction and pattern recognition methods [8].

The study aims to determine the effectiveness of a fast gas chromatography (GC) e-nose which is used to

determine the storage time and internal quality changes during the storage of hen eggs. 3 experiments were conducted: egg volatile detection, internal quality measurement, and sensory evaluation. Yolk and albumen color, spread ratio, freshness, and overall acceptability were the evaluated sensory characters. The fast GC e-nose consists of a sampling system (HS100 autosampler), a detector system connected to 2 flame ionization detectors (FID), and a data acquisition and processing system. Observations showed that haugh unit values decreased as the storage time increased due to a decrease in albumen height. Principal component analysis and Discriminant Factor Analysis were further used to process the data. These confirmed the difference in volatile profiles of egg samples and accounted for a total variance of 95.7% and 93.71%, respectively. Thus, it was concluded that the fast GC e-nose can be used as a reliable instrument for determining the prediction and quality assessment of egg freshness, especially during the supply-chain phase [12].

3. BLOCK DIAGRAM

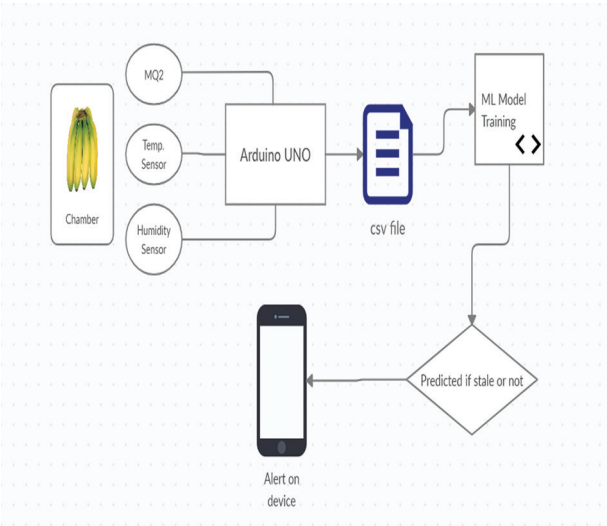


Fig. 1. Block Diagram

4. IMPLEMENTATION

Being a novel idea, there were not any datasets readily available that were structured or could be structured as per our requirement. So, we decided that we would be building a dataset on our own using a banana and a few sensors. The stages of implementation are explained below.

4.1. PROOF OF CONCEPT

The traditional E-noses available in the market are either too expensive, inefficient, and difficult to use. Hence, the first stage involved developing a cost-effective version of the e-nose. After thorough research, the MQ2 sensor, a metal oxide semiconductor was used to test the food products for gas level concentrations (mainly ethylene).

The MQ2 sensor is conventionally used for smoke detection. However, we observed and identified that it is highly sensitive to combustible gases. Concentrations of the gas are measured using a voltage divider network present in the sensor. This sensor works on 5V DC voltage. It can detect gases in the concentration of range 200 to 1000 ppm. This sensor contains Ceramic coated with Tin dioxide, enclosed in a stainless-steel mesh. The sensing element has six legs attached to it, two of which are responsible for heating the sensing element and four are used for output. Oxygen gets absorbed on the surface of sensing material when it is heated in air at a high temperature. The donor electrons present in tin oxide are attracted towards this oxygen, thus preventing the current flow. The ethylene gas from the banana reacts with these oxygen atoms, thereby decreasing the surface density of absorbed oxygen. Current can now flow through the sensor which generates the analog voltage values. This voltage value is an indicator of the concentration of the ethylene gas. A higher concentration of the gas results in a higher analog voltage and vice-versa.

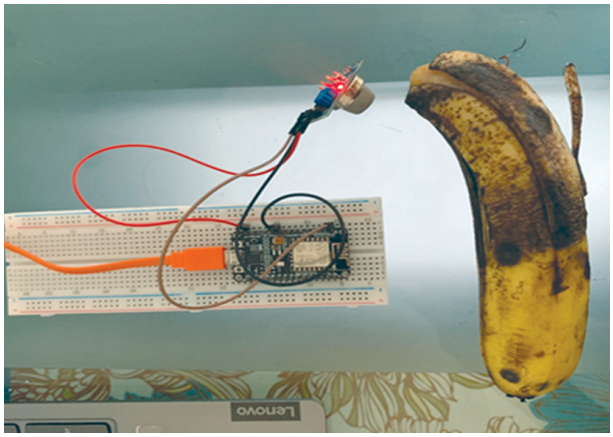
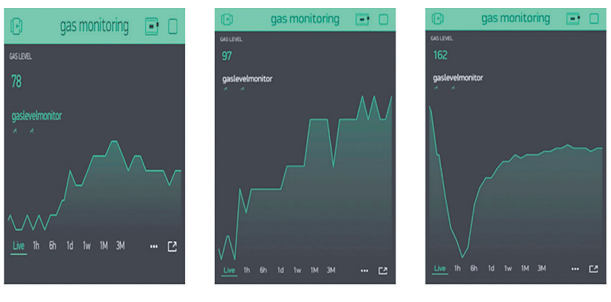


Fig. 2. Proof of Concept Stage

ESP8266 was used to interface the MQ2 gas sensor array with the Blynk IoT application to observe the data in real-time. A banana was put under test and the gas concentrations released by the banana as it continued to ripen were observed. With an increase in time, the gas concentrations increased significantly thus proving that the MQ2 sensor could be used to develop a cost-effective version of an E-nose.



DAY 1 : GAS LEVEL AT 78 DAY 2 : GAS LEVEL AT 97 DAY 3 : GAS LEVEL AT 162

Fig. 3. Graphs for day 1 to 3

4.2. SAMPLING CHAMBER

The gas chamber is an enclosed, air-tight, and controlled environment where the food products have been tested. The chamber must be cleaned at regular intervals with a clean cloth. The controlled environment ensured accurate data collection and reduced fluctuations. It is essential that the chamber remains airtight as outside parameters can severely affect the operating conditions and working of the sensor which is highly sensitive. The gases accumulated in the chamber must be released after every testing interval. The temperature and humidity data are collected using DHT11 sensor that is important to get higher accuracy in the machine learning stage by providing additional attributes.

The gases being released from the product get accumulated in the chamber over time, aiding in the ripening of the food products. Thus, as observed in the 'proof of concept' stage, the gas concentrations being released from the banana keeps on increasing exponentially. Based on this observation, concerned individuals must release batches of their products to ensure that the rest of the product remains fresh.

4.3. DATA COLLECTION

The MQ2 gas sensor is interfaced with an Arduino Uno Board as it is highly compatible and easy to code using C Language on Arduino IDE software. The Arduino Uno reads the analog output voltage at one of its pins, connected directly with the gas sensor. The temperature and humidity sensor, DHT11 was also connected and calibrated to the Arduino analog pins using a similar procedure. This ensured constant monitoring of the room conditions and took into consideration both temperature and humidity, in real-time. 3000 samples over a period of 2 days were taken at a rate of 30 seconds per sample.

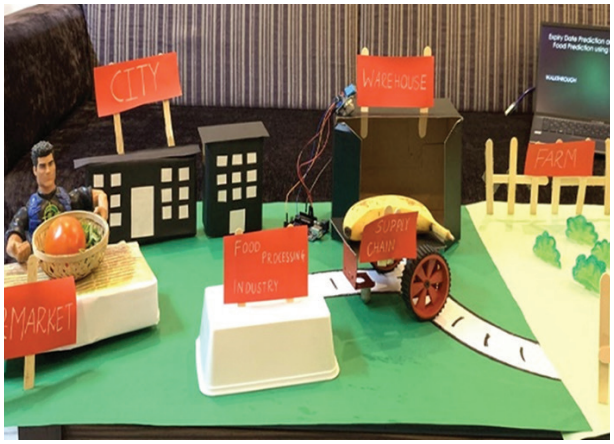


Fig. 4. 3D Model Implementation

4.4. DATA PREPARATION

An unripe banana was taken and placed inside the chamber. The MQ2 gas sensor, also placed inside the compact chamber, was activated by supplying a 5V DC supply through an Arduino module. Similarly, the temperature and humidity sensors were connected and calibrated to the Arduino board. The gas sensor was heated for a few minutes before we started to take the readings. The data from the sensors were captured every 30 seconds. Using the comma as the delimiter, the values were printed onto the serial monitor of an application named Teraterm, which directly logged the data into a CSV file. After repeating this procedure multiple times at different hours of the day, sufficient data had been created in different CSV files. All the CSV files were then merged with their matching columns to create one huge dataset that could further be used for training our machine learning model.

Metal Oxide Semiconductor (MOS) uses a simple voltage divider network. When the gas comes in contact with the sensing element made of Aluminum Oxide (Al2O3) and coated with Tin Dioxide (SnO2), the resistance of the voltage divider network changes in proportion to the gas concentrations. In a clean environment, the electrons in the tin dioxide layer are attracted towards the oxygen present on the surface of the sensing material. However, oxygen present on the surface decreases as they react with certain combustible gas particles thus allowing the donor electrons to become free and allowing a flow of current through the sensor.

MOS sensors operate in the temperature range of 200 to 400°C. These sensors are highly reliable, stable, sensitive, and have a long lifetime. These can be operated in the wide temperature range of -40°C to +70°C and humidity range of 0 to 100%RH. They have a short response and recovery time and do not require heavy maintenance.

4.5. PROPOSED SYSTEM

We have used python for data handling, data preprocessing, and training our model. Google Collaboratory with a GPU-based runtime environment was utilized to write and execute our python code. To work with the imported CSV file, we used common python libraries. First, we converted the CSV file into a data frame using the Pandas library. One of the datasets which contain 3000 data points is displayed in Table 1 given below, where we have printed only the first 10 values (head) of the dataset for initial analysis. We can see the data frame consists of 4 features: gas concentration (in ppm), temperature value, and humidity values are the input features whereas the last column (overripe/ripeness) is the target value that needs to be predicted by our model. Additionally, we used the seaborn library for plotting and visualizing the data we had acquired which helped us gain some useful insights. The graph plot for gas concentration value can be seen in Fig. 6.

Table 1. Data Frame (first 10 data points)

	Different Features/Parameters present in Dataset			
Index	Gas (ppm)	Temperature	Humidity	Ripeness
0	0.083333	0.456405	0.791574	0
1	0.083333	0.627228	0.595237	0
2	0.083333	0.598781	0.599076	0
3	0.083333	0.422635	0.702421	0
4	0.083333	0.618524	0.829969	0
5	0.083333	0.247694	0.752487	0
6	0.083333	0.568728	0.688531	0
7	0.083333	0.470279	0.785262	0
8	0.083333	0.520554	0.839753	0
9	0.083333	0.616535	0.689238	0

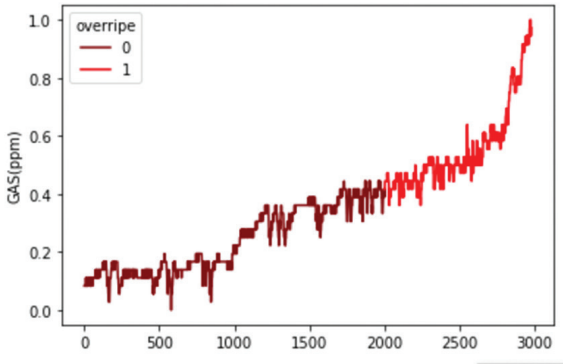


Fig. 5. Gas Concentration Plot

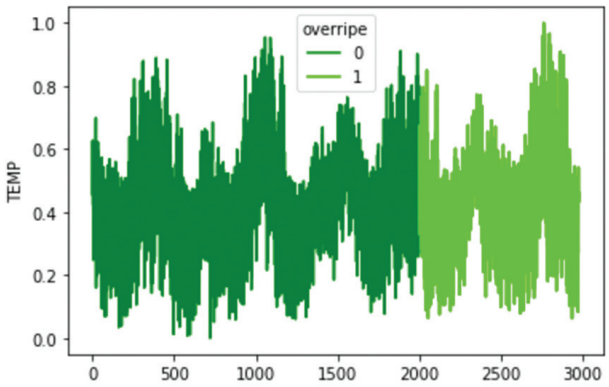


Fig. 6. Temperature Variations

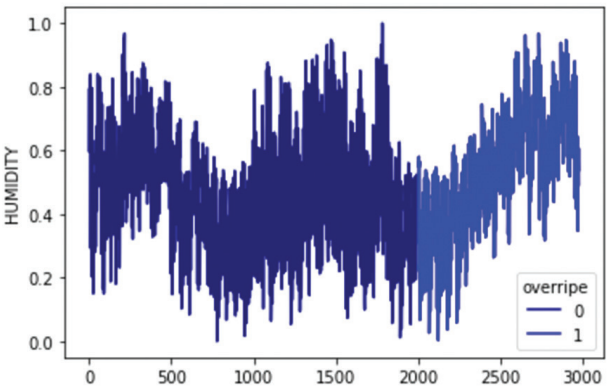


Fig. 7. Humidity Variations

4.6. STATIONARITY

The gas concentration value is non-stationary as it keeps on increasing with time. Whereas the humidity and temperature values are stationary and periodic as the values kept on oscillating between a particular range of values. We can also observe that the gas concentration value starts to increase exponentially after a certain threshold as there is an increase in the emission of ethylene gas as the fruit starts to ripen.

4.7. DATA CLEANING (PREPROCESSING)

By observing the data plot, some outliers can be seen present in the line-plot because the gas sensor is sensitive to temperature and humidity changes. The values which created abrupt changes and disturbed the uniform linear growth of the gas concentration were termed as outliers and removed from the dataset. Secondly, when the fruit is unripe there is no significant change in the concentration leading to a flat graph. Hence, we decided to discard the starting values till they did not begin to show significant changes.

4.8. MODEL TRAINING

For shuffling and splitting the dataset, creating, and training our machine learning model, and finally calculating the accuracy of the different models, we used the Scikit learn module which has multiple libraries available to carry out these functions. The dataset was shuffled randomly so that range of values is properly distributed before splitting it to the training set (75%) and test set (25%). As the numerical features like gas concentration, humidity and temperature have a different range of values, to avoid bias in the data, we used StandardScaler (a Sklearn library) to scale the data to a given range. It can be inferred from the given table below, Logistic regression, Decision Tree Classifier, Support Vector Classifier (SVC) & K-Nearest Neighbours (KNN) classifier were the different models trained and tested on our data. We achieved the highest accuracy of 97.05% on the Support Vector Classifier model.

4.9. DATA COLLECTION

The traditional E-noses available in the market are either too expensive, inefficient, and difficult to use. Hence, the first stage involved developing a cost-effective version of the e-nose. After thorough research, the MQ2 sensor, a metal oxide semiconductor was used to test the food products for gas level concentrations (mainly ethylene).

5. RESULTS

5.1. RESULT TABLE

Following is the accuracy and ROC_AUC score obtained for different machine learning models. Accuracy Score column measures how many observations, both ripe and unripe, were correctly classified.

ROC AUC Score tells us how good our model is by calculating the Area Under the ROC Curve (Refer Fig. 4). More top-left the ROC curve is, the higher the area and hence we will get a higher ROC AUC score.

Table 2. Accuracy and ROC AUC Score of different models

Machine Learning Model	Accuracy Score	ROC AUC Score
Decision Tree Classifier	96.51%	0.992
Gaussian Naïve Bayes	91.3%	0.987
KNN Classifier	95.97%	0.989
Logistic Regression	96.78%	0.995
Support Vector Classifier	97.05%	0.996

5.2. LEARNING CURVES

The learning curves are computed to choose the perfect ratio to split the dataset into training and testing sets, to minimize the error, improve the accuracy of the model and allow to detect of high variance or high bias is present in the data. After careful evaluation of the learning curves, the dataset was split with 75% of the data as a training set and 25% as the test set.

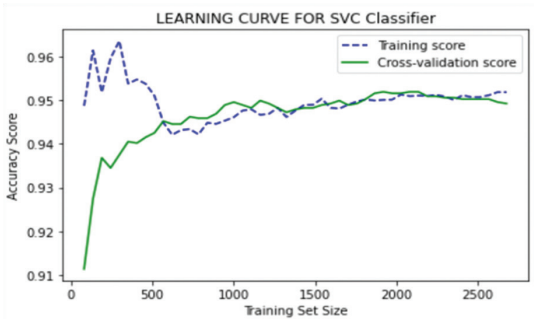


Fig. 8. Gas Concentration Plot

5.3. ROC CURVES

The Receiver Operating Characteristic curve (ROC) curve is a useful tool for predicting the probability of a binary outcome, which plots the false positive rate (x-axis) versus the true positive rate (y-axis) for different candidate threshold values between 0.0 and 1.0. ROC curves are to be used when the observations are balanced between each class.

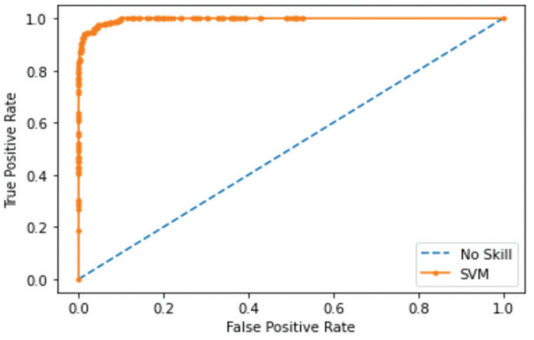


Fig. 9. The curve for SVM Classifier

5.4. CONFUSION MATRIX

The confusion matrix represents the number of correct and incorrect predictions made by the classifier, thereby evaluating the performance of the classification model. The matrix is displayed in the form of a heatmap.

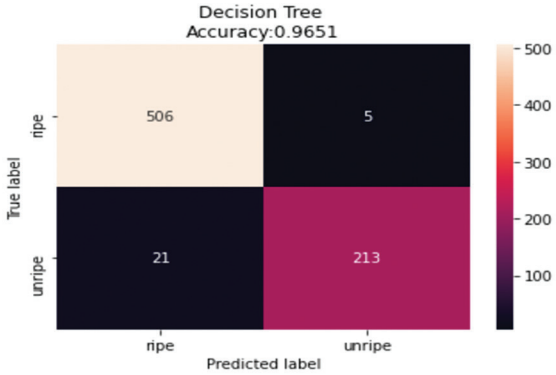


Fig. 10. Confusion Matrix

6. CONCLUSION

Technologies like the Internet of Things (IoT) and Machine Learning have been used in this project to accurately determine the expiry date of food products to reduce food wastage. To achieve this, a cost-effective version of a traditional e-nose was developed and used for the detection of staleness of food products. The gas level (ethylene) was mapped and recorded for different ripening stages and a data set was recorded successfully using a banana. After the data collection, data cleaning (prep-processing steps) was implemented. Further, machine learning algorithms like Logistic regression: 96.78%, Decision Tree Classifier: 96.51%, Support Vector Classifier (SVC): 97.05% & K-Nearest Neighbours (KNN) classifier: 95.97% were used to process the data and gain valuable insights regarding the ripening stage and expiry date. These results proved that this low-cost e-nose, supported by efficient machine learning algorithms can be used to determine the expiry date and reduce food wastage.

7. FUTURE SCOPE

The project model used and discussed in this paper can be extended to work with any food product that emits incremental amounts of ethylene gas or other volatile gases during its ripening stages. The current sensor-based system can be enhanced by using Raspberry Pi and camera-based model. The camera can be used to detect the color and texture of the food item while the R-Pi will provide additional processing capability. The machine learning models mentioned above are only being used as a binary classification algorithm to predict if the food item is getting stale or not. It can be further enhanced by utilizing a time-series forecasting model which can show accurate expiration dates of products

beforehand. The prototype can be made compact and easy to use by individuals in different industries like food processing, supply chain, and farming. It can be used to raise awareness among people about the accurate expiry date of their food products. We also want to provide suggestions on the accurate way to utilize/dispose of their food products, for example, if it has reached an over-ripened state, the suggestions regarding composting will be provided to the user via a mobile notification, thus ensuring that the food is not wasted, but utilized optimally.

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Legacy Digital Transformation: TCO and ROI Analysis

Review Paper

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Abstract *– Legacy Digital Transformation is modernizing or migrating systems from non-digital or older digital technology to newer digital technologies. Digitalization is essential for information reading, processing, transforming, and storing. Social media, Cloud, and analytics are the major technologies in today's digital world. Digitalization (business process) and Digital Transformation (the effect) are the core elements of newer global policies and processes. Recent COVID pandemic situation, Organizations are willing to digitalize their environment without losing business. Digital technologies help to improve their capabilities to transform processes that intern promote new business models. Applications cannot remain static and should modernize to meet the evolving business and technology needs. Business needs time to market, Agility, and reduce technical debt. Technology needs consist of APIs, better Security, Portability, Scalability, Cloud support, Deployment, Automation, and Integration. This paper elaborates different transformation/ modernization approaches for Legacy systems written in very long or End of Life (EOL) systems to newer digital technologies to serve the business needs. EOL impacts application production, supportability, compliance, and security. Organizations spend money and resources on Digital Transformation for considering Investment versus Return on Investment, Agility of the System, and improved business processes. Migration and Modernization are critical for any Legacy Digital Transformation. Management takes decisions to proceed with Digital Transformation for considering Total Cost Ownership (TCO) and Return on Investment (ROI) of the program. The paper also includes a TCO-ROI calculator for Transformation from Legacy / Monolithic to new architectures like Microservices.*

Keywords*: Legacy, Digital Transformation, Automation, Migration, Modernization, Monolithic, Microservices*

1. INTRODUCTION

Organizations are currently investing money and resources in transforming their existing systems into feature-ready digital technologies. Each has a different business strategy to grow. They are adopting Digital Transformation by planning and implementing new digital systems for business changes in the Organization with employees' participation. Transformations help the Organization lower the operating cost considerably by adopting automation, innovation, and creativity rather than traditional methods. The best example of Digital Transformation is cloud computing in the Organization, which reduces the owned hardware cost and maintenance and increases the trust in subscription-based models. Digitalization provides opportunities to transform business models, consumption, legal and policy measures, and cultural barriers. Renovating and optimizing business processes is the success of digital Transformation. Organizations must factor in the cultural changes concerning workers, and organizational leaders adjust to adopting and relying on unfamiliar technologies while planning for the Digital Transformation strategy. The revenues, profits, and opportunities increase upside after Transformation

completes. Lack of innovation impacts the business's long-term competitiveness and profits. Automation also plays a critical role in increasing Business efficiency and Agility up to 50-60%. EOL also a significant objective for migrating the applications to a new technology stack. The majority of the software EOL ranges from 10-15 years. Major domains involved in Digital Transformation were Hospital Management, E-Commerce, Banking, Insurance, Training, Education, and Health care.

Legacy-based applications constantly face challenges like high maintenance and upgrades cost, unsupported hardware, resource cost, flexibility, scalability, and integration to the external system. Legacy application is an IT-critical day-to-day operations system build on outdated technologies. Several applications are running for the last 20-30 years in the world with legacy technologies. The applications use mainframe and other 3GL languages for core business operations. Many companies continuing legacy systems regardless of the age and technology of the application used. Such legacy applications' running cost is very high in maintaining and support—time to modernize such applications with proper planning and strategy. Legacy modernization is also called software or platform modernization. Legacy Modernization approach consists of two major phases called the Assessment phase and Implementation phase. Organizations are migrating their existing legacy applications to modern technologies with the help of microservices architecture patterns [28] [24] [22] [18] [15]. Microservices architecture promises high maintainability for software modernization [30], including decomposing the application into microservices-based on experience. Concluded due to higher efforts, the process is viable for large migrations and complex systems with high business value.

This paper organized as follows: Section II we describe Literature Review, Section III we describe Modernization Approaches, Section IV describes TCO_ROI Analysis, and Section V Concludes the paper

2. LITERATURE REVIEW

This section describes the literature review of the work done in this area. The research carried out [1] digital transformation capability maturity model on staged way using science research approach. Decomposition method [2] for migrating monolithic to microservices applications. Identify similar semantically operations and cluster together for a microservice. Evaluation metrics used to identify the right microservices candidate. Legacy system challenges [3] highlight along with solutions. The proposed legacy modernization uses Rehosting, Replacing, Mitigation, Retargeting, Revamping, Wrapping, and Program translation. Systematic [4] review was conducted on legacy system modernization papers and concluded the importance of integrating quality. Explains different modernization types as Complex migration, increased migration, and partial migration and compared the modernization strategies like partial migration, complete migration, and wrapping. System Migration Life Cycle [5] proposed for step-by-step migration strategy from legacy to cloud platforms. Framework includes three stages – pre-migration, migration, and post-migration. Studied [6] the cultural readiness of the executives is important. Studied [7] different papers on legacy migrations and identified the factors – Process Aspects, Human Aspects, and Organization Aspects. Proposed 5 phased migration approach called Plan for Modernization, System Requirement Gathering, Design & Development, Testing, and Execution. Explains [9] what next in the FinTech industry after Digitalization using AI, Blockchain, Quantum computing, IoT, and Smart contracts. Explains disruptive innovations in trading, crypto, and monetary in FinTech systems. Proposed different process to [8] [12] [13] identifying the microservices from monolithic applications and uses of blue-green [10] strategy for faster deployment.

Conducted survey [11] with specialists to identify valuable criteria for identifying microservices from legacy systems. Use of Architectural Trade-off Analysis Method [14] for Architecture evaluation of old legacy system. The proposed [15] architecture strategy around business functionality concepts comprises 5 phases – Functional analysis, Business functionalities identification, Business functionalities analysis, Business functionalities assignment, and Microservice creation. [16] [17] [21] [29] case study and survey conducted for migrating monolithic to microservices for large-scale industries to identify issues, solutions, challenges, strategies, and risks. VUCA [20] explains how the digitally immature organizations in the COVID pandemic. VUCA, acronym of Volatility, Uncertainty, Complexity, and Ambiguity to identify the unpredictable external environments. Concludes that COVID made digital transformation for all businesses and all sectors. Explains [22] three challenges for legacy migration to microservices are Multitenancy, Stateful, and Data Consistency. The three challenges addressed in microservices to develop stateful systems, implement multitenancy systems, and solving data consistency issues Proposed [23] reference model for Digital Transformation (DT) applications using Business process Management Contextual Factors and DT. Presented [25] lessons learned during migration - functional approach, norms and standards, microservices granularity, and integration outcomes are critical aspects described in the paper. Serverless compute architecture [26] [32] was proposed for migrating monolithic applications with benefits. Suggested boundary context approach [31] that extends static and dynamic analysis for decompositions of microservices. Recommended algorithm approach [33] for extracting microservices migration.

Introduced generic model [40] allows incorporating the characteristics of relevant dynamics that instantiated for specific characterizations. Studied [35] 20 migration techniques from literature, and results show that DB migration is the challenge. Address [37] migration issue by adding two questions – the cost of decomposition and

domain entries. Conducted survey [38] on motivational drivers for migration and concluded maintainability and long-term returns are primary factors. Reported [42] open-source research on modularization and modernization process. The process decompositions of web as well as technical components. Adopted CORAL (Collaborative Reengineering and Modularization Approach) for modernization process from legacy to microservices. Presented [36] high available application use case for ticket booking application modernization to microservice architecture and identified several benefits – choose preferred technology, no dependency on hardware, and new feature enablement using DevOps. Presented real-world financial case study [18] to demonstrate scalability by migrating monolithic to microservices architecture. Technical problems addressed using repeatable migration process adoption in Danske Bank legacy application to microservices architecture. The reengineering approach discussed reduced complexity, lower coupling, higher cohesion, and a simplified integration. Technical lessons [24] learned discussed as part migration process in MGDIA SA company spending around 3 years with 17,300 person-days. Demonstrated the Return on Investment for the migration with an Increase in Revenues, Replacement facilitated, Performance increase, and lower level of support. The proposed [28] candidates to show the relationship between extracted and whole structure. Analyze the relationships between program groups and data for preparing microservices.

3. MODERNIZATION APPROCHES

Legacy Modernization approach consists of two major phases - The assessment phase and the Implementation phase. The assessment phase consists of IT portfolio Assessment, To-Be Architecture definition, modernization strategy, and business case justifications. The implementation phase considers modernization Application Transformation, Database Transformation, Infrastructure Transformation, and Operational Transformation. Below are the challenges considerations while modernizing the applications

- Lack of portfolios across applications
- Poor management of systems documentation
- Large application maintenance
- Cost and duration of modernization
- Legacy and new systems coexistence
- Commitment from stakeholders
- Adoption of new technology platforms
- Cultural change adoption
- Adopting a new way of working (E.g., Work from home options)
- Retain and enhance the application with business needs
- Business value and ROI

Application Modernizations is not a rewriting of code from one technology to another. Following principles has to take into consideration while doing modernizations.

- Clear Organization road map to get early ROI
- Developing new capabilities
- Adoption of Open standards rather than vendor lock-in
- Adoption of microservices design rather monolithic
- API version support for all service calls
- Use of integration layer for seamless external system integrations
- Identify new business channels and models to build new digital channels
- Balance between Business and Technology for time to market
- Effort and cost optimizations
- End-user OR customer delight
- Adoption of Agile and DevOps

Good architecture, design and coding, vendor-neutral, maintain open standards, and security compliance with measurable KPIs are the critical factors for successful application modernization. The assessment phase recommends the applications have to be Retain, Retire/Rationalize, Rehosting, Replace, Refactor, Re-architecture, and Rebuild / Rewrite (7-R's). Based on the assessment recommendation, the transformation strategy derives as per the Organization's goals. Legacy Applications categorization is based on the number of users, criticality, benefit, maintenance cost, risk, and feasibility. Reactor or Rewrite's legacy application decision is to study existing source code analysis and understand cloud-native compliance based on 12-factor anti-patterns and categorize applications. Adopt Agile and DevOps for a new way of working in the digital world. Table-1 describes each modernization approach with their benefit.

Application Modernization has several options from Legacy to new Digital. Below are the top modernizations options

- Legacy to Open platforms
- Legacy (Cobol / native languages) to Microservices
- Monolithic to Microservices
- Commercial to Open-Source

Application modernization/migration done manually and tool-based.

Tool-based migration approach - Conversion tool to automatically convert the existing use cases into the target technologies to whatever extent the tool can support and then hand-finish the code to adhere to the "as-is" functionalities as shown in Fig 1. Migration tool to convert the existing use cases into target platform, and this option typically has two-step processes:

- Tool based conversion (up to 60-80% conversion)
- Hand finishes the missing content by the tool

Modernization Approach	Scenarios to Fit	Benefit
Retain	Retaining the application as-is without adding any new features	No change in TCO and business value
Retire/Rationalize	Applications no longer in use. Merge the functionality to another application.	Reduce Total Cost of Ownership with rationalization of applications
Rehosting	Deploying the applications in a Virtual / Cloud environment without any change	Reduce migration cost and operations.
Replace	Eliminate existing application components and functions with new requirements.	Lower the operational cost with compared to Legacy application
Refactor	Standalone applications needs interfaces using modern technologies without modifying features and functions	Reduces Total Cost of Ownership and Improves maintainability
Re-architecture	Shift the application to new platform architecture with better capabilities	Improves the non-functional capabilities
Rebuild / Rewrite / Reengineering	Rewrite the application components with new technology stack without changing the scope and functionality	Flexibility to customize as per business needs

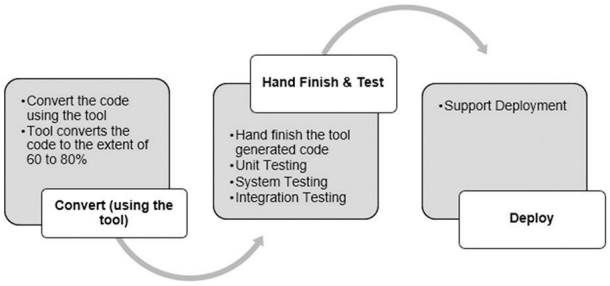

Fig. 1. Tool based migration approach

Manual migration approach – Consists of reverse engineer the existing technology stack requirements and rewrite manually into target technologies covering the entire SDLC phase of Design, Development, and Testing. Reverse engineering methodology is a two-step process called reverse engineering followed by forward engineering, as shown in Fig 2. Study the existing applications and collect the business rules, design models, and workflows and document as part of reverse engineering. After done the reverse engineering, build the new application on the target platform using the documentation.

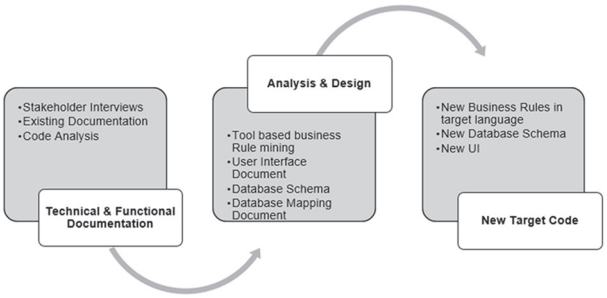

Fig. 2. Manual based migration approach

Table 2. Manual and Automation migration comparisons

Parameter	Manual Migration	Automation Migration
Cost	High	Low
Schedule / Time	Longer Development Cycle	Shorter Development Cycle
Code Quality	Sometime not clean and good	Clean and good
Flexibility	Maximum flexibility in design and modification	Very rigid, based on rules defined in the tool

Legacy modernization has many benefits in terms of reduced cost, enhanced flexibility, and vendor options. Nowadays, the modernizations are widespread, from Legacy to Cloud-ready, DevOps, Automation, AI and Big Data, and Mobile First approach application. Migrating legacy applications to Cloud for better scalability, performance, and flexibility. DevOps simplifies the process of modernization by shared responsibility and a collaborative approach. Manual processes are the barriers to the Legacy applications. Organizations can reduce operational costs and increase efficiency by moving manual to automation. Digital Transformation uses AI-based tools for Data-driven decisions. Mobile-first approach development leads the business to serve the customer in a faster and flexible manner.

4. TCO-ROI ANALYSIS

TCO and ROI analysis help the right investment decisions for digital transformations. TCO is a cost spent OR One time cost spent for the modernization of the systems. Return on Investment is the ratio between investment gains and TCO. Application is migrating to Cloud the cost distributed among several years for hardware and software. The below use case provides details of TCO-ROI calculation for commercial to open-source transformation.

Calculate the cost incurred for the current environment concerning application scopes described in Fig 3 – Hardware, Operating System, Web & Applications Servers, Database Servers, Application Maintenance, and Other Integration Systems. Fig 3 provides the information about current environment cost

Application Scope	Ontime Cost	Support		
		Year 1	Year 2	Year 3
Hardware Cost				
Operating System	$20,000.00			
Web & Application Servers (Commercial)		$20,000.00	$20,000.00	$20,000.00
DataBase Servers (Commercial)		$20,000.00	$20,000.00	$20,000.00
Applications Maintenace		$10,000.00	$10,000.00	$10,000.00
Overall Hardware Cost	**$20,000.00**			
Overall Software and Maintenance Cost	**$20,000.00**	**$50,000.00**	**$50,000.00**	**$50,000.00**
Overall Cost	**$40,000.00**	**$50,000.00**	**$50,000.00**	**$50,000.00**

Fig. 3. Current environment Cost

Calculate the one-time cost incurred for new environment concerning application scopes described in Fig 4 – Hardware, Operating System, Web & Applications Servers, Database Servers, Application Maintenance, Other Integration Systems, Migration Cost (Modernization efforts and time), Decommission cost, Parallel Run cost, and Maintenance. Fig 4 provides information about the new environment cost after migration.

Application Scope	Ontime Cost	Support		
		Year 1	Year 2	Year 3
Hardware Cost	$40,000.00			
Operating System (RedHat Linux)	$20,000.00			
Web & Application Servers (Open Systems)		$200.00	$200.00	$200.00
DataBase Servers (Open Systems)		$200.00	$200.00	$200.00
Migration Cost	$10,000.00			
Training Cost	$2,000.00			
Other productivity impact cost	$100.00			
Decommissioning cost	$100.00			
Parallel Run cost	$50.00			
Applications Maintenace		$8,000.00	$8,000.00	$8,000.00
Overall Hardware Cost	**$60,000.00**			
Overall Software and Maintenance Cost		**$8,400.00**	**$8,400.00**	**$8,400.00**
Ontime Migration Cost	**$12,250.00**			
Overall Cost	**$72,250.00**	**$8,400.00**	**$8,400.00**	**$8,400.00**

Fig 4. New environment Cost

ROI calculated based on the one-time investment shown in Fig 5.

ROI Consolidated				
	One time Cost	Year 1	Year 2	Year 2
Overall Cost - Current Environemt	$40,000.00	$50,000.00	$50,000.00	$50,000.00
Overall Cost - New Environemt	$72,250.00	$8,400.00	$8,400.00	$8,400.00
Total Savings		$41,600.00	$41,600.00	$41,600.00
Total Investment	**$32,250.00**			
Return on Investment		**$9,350.00**		

Fig 5. ROI Calculation

Return on Investment (ROI) = Overall Cost (Current Environment) – Overall Cost (New Environment)

From the above Fig 5 the Total Investment (TI) = One-time New Environment Cost – Current Cost (Software + Environment)

Total Investment
= $ 72,250.00 - $ 40,000.00 = $ 32,250.00

ROI Year-1 = Current Environment Cost (before migration) – New Environment Cost (after migration)

ROI Yeat-1 = $ 60,000.00 - $ 8,400.00 = $ 41,600.00

If the value is positive in Fig 5, the new environment maintenance cost of the product is less compared to the Old environment. Compare the overall cost between current and new environment. In the above case study, the difference between the new environment's one-time cost and the current environment is $32,250.00. Investment made by the modernization of the application to a newer environment. From Year-1 onwards, the saving from New and Current environment is around $41,600.00. The Return on Investment made in the first year of the modernization.

Sometimes applications are digitalizing to new technology stack to support new business. Banking industry enabling of Mobile for the existing application to invest some amount to get ROI with the time frame. The ROI analysis helps the management team to identify the applications to be migrated first.

5. CONCLUSION

Legacy Digital Transformations are essential nowadays for Organizations to enabling the time-to-market in their business. While making any decisions on transformation or modernization, management has to calculate the TCO-ROI of the program. ROI calculation helps the Organization to spend the time and efforts in the right direction. Sometimes the ROI calculation is not direct and has to develop logic how much revenue growth performs for the new feature. The ROI has to return from 2-3 years, and then the TCO spend is perfectly utilized. The right R (Retain, Retire/Rationalize, Rehosting, Replace, Refactor, Re-architecture, and Rebuild / Rewrite) approach has to choose while performing Digital Transformation consideration Agility using DevOps. The modernization program has to complete as per business agility. This paper highlights the TCO-ROI factors for any transformation or modernization, which influences the modernization strategy. There is scope to identify new transformation approaches for the newer business needs and technology transformations.

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Appointment scheduling system in multi doctor/multi services environment

Case Study

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Abstract *– Appointment scheduling systems are used by health care providers to manage access to their services. In this paper an algorithm and a web application for automatic appointment scheduling is presented. Both are implemented using the concept of booking appointments for patients for a specific service offered by each doctor. The purpose of the application is to make signing up for a specific service easier for patients and to improve health tourism in Croatia by maximizing doctor's efficiency and minimize patient waiting time. Medical providers are added to the system, they add the services which they provide, and each service offered has its own duration time. Users register, search for services matching their parameters, and schedule an appointment for the requested service. Available appointments are generated using the presented algorithm, which is the main part of this paper. The algorithm searches the database and returns possible appointments. If patient has more than one appointment, possible appointments time can be before the existing appointment, between two appointments, or at the end of the last appointment. Thus, web application enables the patient to reserve desirable appointment time.*

Keywords *– scheduling algorithm, health tourism, medical organization, web application*

1. INTRODUCTION

Internet and mobile applications have become popular and part of our everyday life. Their aim is to make life much more comfortable by providing users with useful information and services in a transparent way. Thus, users do not need to worry about complicated calculations, configuration and scheduling tasks to get appointment for services that they need.

Organization of a medical appointment scheduling systems is a mandatory for an efficiency medical system. To improve healthcare tourism in Croatia, we must ensure timely access to health services for all patients. Timely access is a key factor for achieving successful medical results. It is also an important determinant of patient satisfaction. For a people, the biggest burden is making an appointment and going to doctor's office, because they know beforehand that they will be waiting. If they have more appointments, it is necessary to reduce or completely eliminate waiting time at medical institution. On the other hand, the doctors are busy people and want to use it efficiently. Every time that patient is late on appointment or just does not come, doctors schedule will be empty and unused. In this paper, we are focused to reduce doctor's idle and overtime.

Organizing an appointment in office with only one doctor is a complex task. First, one of the patient scheduling models must be selected [1-3]. However, without additional information, such as the patient's medical history, the patient's condition, whether it is a first or follow up visit, or some other reason, it is difficult to determine the duration of the examination. Consequently, organizing and ordering patients in a multi doctor/

multi services environment is more demanding task than in office with only one doctor.

The focus of this paper is to present algorithm for organization and automatic appointment scheduling of patients in multi doctor/multi services environment. It does not consider problems pertaining to the size of staff and facilities or with resource allocation in multiple-service-site systems like in [4]

2. SCHEDULING ALGORITHM

In this paper algorithm for automatic appointment scheduling in multi doctor/multi service environment is presented. We observed different approaches and combined them to get final algorithm which suits for such environment. Our algorithm uses the usual block schedule similarly as in [5, 6]. In these studies, authors use analytical methods instead of simulation to estimate performance. Some other studies use a dynamic programming approach to determine the optimal variable-sized multiple-block schedule approaches [7-9]. Another study [10] suggests heuristic approach in which service time depends on the relative position of the service in the schedule. In other study [2] simulation-based techniques are used to measure the performance Appointment scheduling algorithm in health care using variety of heuristic appointment rules. Another approaches use genetic algorithms and machine learning for patient scheduling in highly constrained situations [11].

Our algorithm is combination of heuristic, dynamic programming and genetic approach. The construction of an automated scheduling algorithm is complex task because there is need to schedule human resources. But manual scheduling takes a lot of time and many administrative work and in some cases is impossible to find solution. The heuristic algorithms are used to find a solution close to the optimal in cases where finding the optimal solution is not possible. These algorithms work by getting closer and closer to the optimal solution as they progress. Their merit is that they can find a solution very close to the optimal solution in a relatively short time. Another approach is dynamic programming which simplifies a complicated problem by breaking it down into simpler sub-problems in a recursive manner. Sub-problems can be solved different programing algorithms.

Genetic algorithms are subgroup of heuristic algorithms and they are used to solve optimization problems. Genetic algorithms use idea of natural selection and genetic processes in the nature. As the nature life evolve using the principles of natural selection genetic algorithms also evolve to resolve problems. For the genetic algorithm knowledge structures, structural changes and the operators which change structure. To change knowledge structures different approaches can be used. The simplest approach parameters change and that changes system's behavior [11]. In our algorithm the most important parameters are the number of patients, number of medical staff, services and available appointments. These parameters determine scheduling quality:

- Appointment duration
- Doctor's idle time and overtime
- Patient's waiting time between appointments
- Total number of appointments is certain period

To improve scheduling quality appointment duration, doctor's idle time and patient's waiting time should be minimized, while the total number of appointments should be maximized. In this paper, parameter change is used for algorithm evolving. If the quality of service is reduced algorithm will change parameters to evolve. For example, if patient's waiting time is too long, the algorithm can reduce the number patients or add more medical staff to the system. If some doctors have many overtime, scheduling algorithm will transfer appointment to less busy doctor. There are many factors that impact on scheduling algorithm and it is impossible to apply them all.

The algorithm is presented using flowchart diagram which is consisted of a series of arrow-related symbols that define the flow and direction of program execution. This algorithm representation is simple, easy to review and easy to find. Problems can be easily analyzed and compared to another problem, which shortens the time to find a solution. In order to find available appointment time, it is necessary to create database for storing data. Database E-R diagram is shown in Fig. 1.

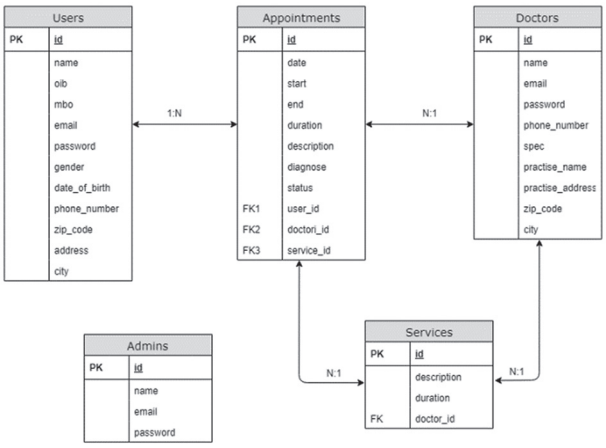

Fig. 1. Database E-R diagram

As shown in Fig. 1. database contains the following tables:

- Users represents the users (patients)
- Doctors represents the doctors
- Appointments represents the scheduled appointments of users with each doctor

- Admins contains information about the application administrators
- Services is providing all possible services offered by individual doctors

User and Appointments tables are related by a 1: N relation, which means that one user can have more than one appointment, while one appointment only applies to one user (patient). Further, the Appointments and Doctors tables are related by a N: 1 link, indicating that one appointment can only refer to one doctor, while one doctor may have multiple appointments. The Appointments and Services table are related by a N: 1 relation, since one appointment can have only one service, while the same service can belong to several different appointments. In addition, the Doctors and Services tables are related by a N: 1 relation, indicating that one doctor may offer multiple services while one service belongs to only one doctor. The Admins table is not related with other tables, but has a separate role. Application is made using PHP framework named Laravel which uses migration to create the tables.

Our algorithm starts by looking for an already reserved appointments and makes them unavailable for future search. When a patient chooses the date range in which he or she would like to book an appointment, it is primarily followed by checking that the selected dates are valid. Also, algorithm searches for patient's already reserved appointments in selected time period to prevent appointment collision. The user can set the start date as early as tomorrow, while the end date could be same as start date, or any other date in future.

The next step is check for existed records in the Appointments table for the selected time period. If there are no records for the selected time period, the user is offered an appointment at the beginning of each day in selected time period. In this paper we used 08:00AM for the beginning of business day. Start time can be changed independently for any medical institution. If there is a record in the database for the selected dates, it is checked when first appointment starts for that day. If the start of the first appointment is greater than 08:00, it means that there are empty time slots before the first appointment of the day, and it is checked can be offered for appointment. In order to be able to offered, it is necessary to check whether the appointment time fits in the empty space until the next reserved appointment. If the condition is fulfilled appointment is reserved for current user.

In case these conditions are not fulfilled, and there is no free time slot before first reserved appointment, algorithm checks are there another free time slots for comparison in the database on the same day. If free time slot is found, it is checked whether the selected appointment ends before 16:00 hours, since it is assumed that is the end of working hours. End time of working hours also can be changed independently for any medical institution. If the condition is fulfilled, appointment is reserved for current user, and if not, it means that the day has been filled and appointment checking will be moved to the next date selected by the user.

Algorithm checks for the next date in selected time period and searches for the free time slot in the same way as for the first day in previous step. After all days are checked and algorithm did not find free time slot, appointment could not be reserved and algorithm has failed. The failure to meet this requirement means that there is not enough free time between start and end date, thus user is prompted to select another time period. The implementation of the algorithm is shown in Fig. 2.

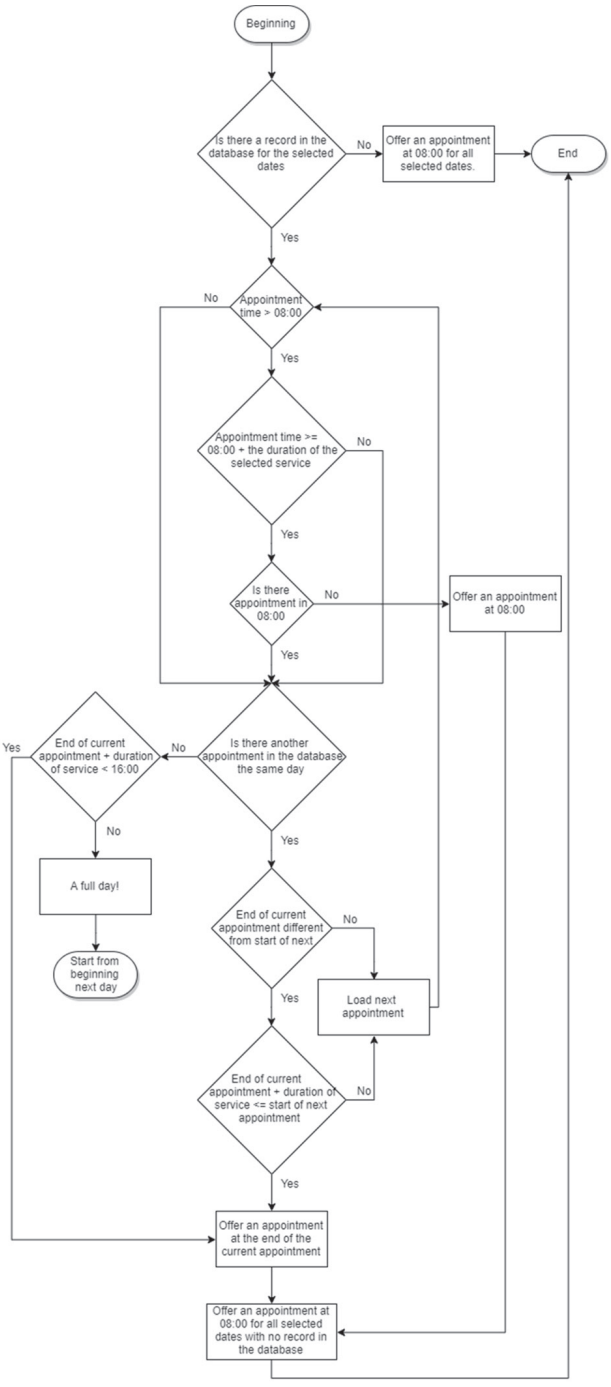

Fig. 2. Block diagram for appointment scheduling

3. APPLICATION

The basic concept of the application is focused on health care tourism and goal is to achieve satisfaction of patients. Application should be user friendly and should ensure easy way to make the appointment. The patient selects the medical institute and the city in which he wants to make an appointment. After selection of medical institute or city all available medical staff are shown to the patient, and by selecting one, patient reserves one of the available appointments that suits him best. In Fig. 3. the homepage of the internet application is displayed.

If they want to book an appointment, patients need to log in with their user information. The patient is logged in by entering the Insured Identity Number and password. In case the patient does not have an account, registration is required. By choosing to register, the form is shown as in the Fig. 4.

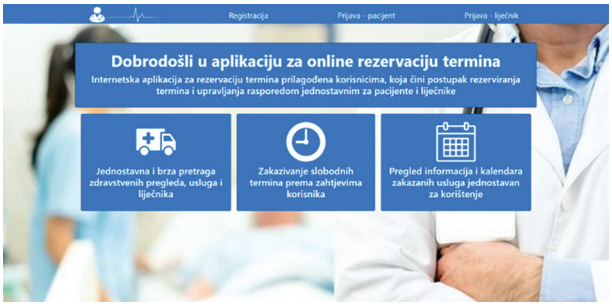

Fig. 3. Application home page

Fig. 4. Registration form

After registration user is redirected to user profile as shown in Figure 5.

Logged patient can search for the medical institution where the appointment (service) is going to be scheduled. The first thing the user chooses is the medical institution and the city where they want to book an appointment. In case the user's selection does not find any result, the user receives feedback and is offered a return to the homepage. In the next step all founded doctors are shown that fit the parameters and their basic information (first and last name, address, email, phone number, office address, etc.). The user selects the doctor who best suits his requirements. After the user has selected the doctor with whom he wants to request a service, then the service itself is selected. The user chooses the service for which he wants to book an appointment. Also, in this booking step patient will see a map with the exact location where the examining office is located as Shown in Fig. 6.

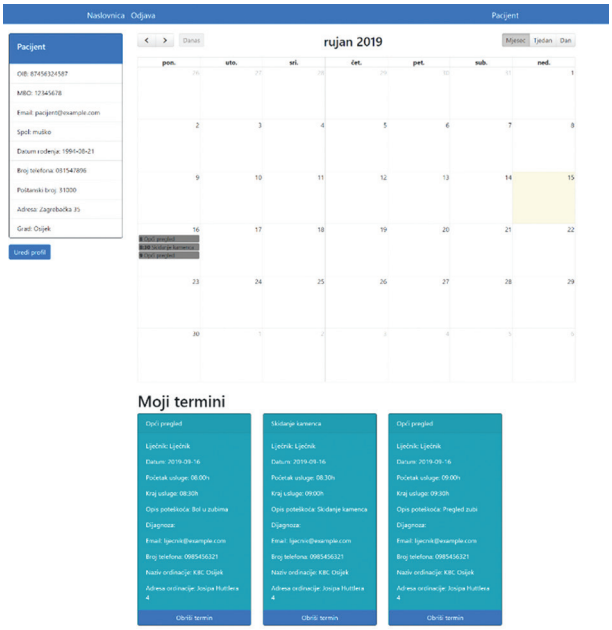

Fig. 5. Patient profile page

Fig. 6. Information about doctor and his location on map

In the next step, it is necessary to select the date range for which the patient wants to see the available appointments, and to choose the one that suits him best. The start date of the range must be one day longer than the current day, since it is not possible to book an appointment in the current day, but no earlier than the next day. In the event that this condition is not fulfilled, the same page is reloaded and the patient is informed to choose another time period. After selecting a valid date range, the algorithm performs its task and returns to the patient the appointment information and process is over.

In addition to being able to sign up for patients, there is also the option to sign up for medical staff who offer their services. The medical staff is not able to register himself, but they are added to the system by the application administrator. When an administrator enters

a new medical staff into the system, they receive a welcome message at the email address with the user name and password that he logs in to. A password is randomly generated when creating account, and only the created account has access to the password. When a doctor or some other medical staff is logged in, a home page opens showing all the available terms of the registered doctor. As with patients, a calendar view of the appointment schedule is set. Below the calendar view, all the reserved appointments of the patients are listed in card form, where it is possible to see the details of the appointment. In addition to scheduling details, below the calendar is a form to add services that the doctor or some other medical staff offers. Selecting the "Add new service" option opens a page where the description of the service offered and the duration of the service itself can be entered. Successful entry reloads the profile listing the services offered. Each enrolled service can also be removed by selecting the "Delete Service" option, located at the end of the name of each service. Doctor's profile with all appointments and services offered are shown in Fig. 7.

In addition to reporting patients and doctors, there is also a way to sign up for a site administrator. Once logged in administrator can see all the medical staff in the database and their information. There are options for each doctor with which the administrator has the ability to edit information and remove the doctor from the database. In addition to existing doctors, the administrator also has the option "Add a new doctor", since doctors do not have the option to register with the system. The admin dashboard layout is displayed in Fig. 8.

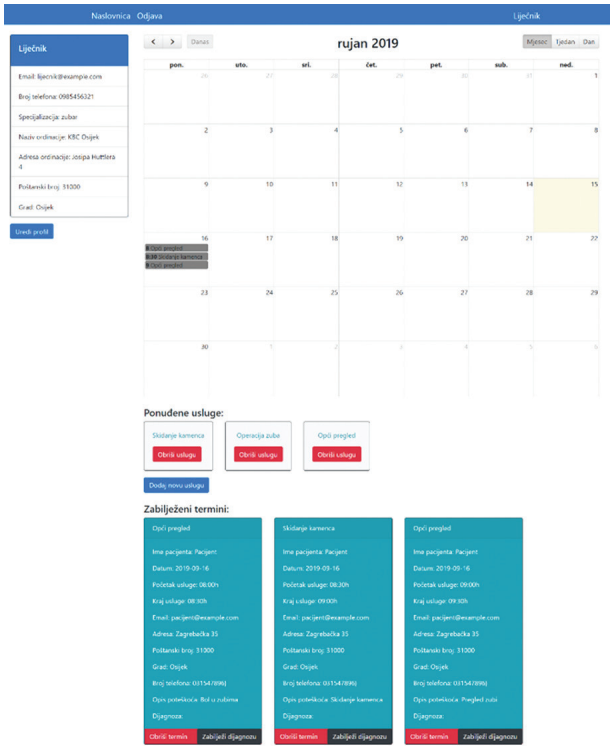

Fig. 7. Doctor profile page

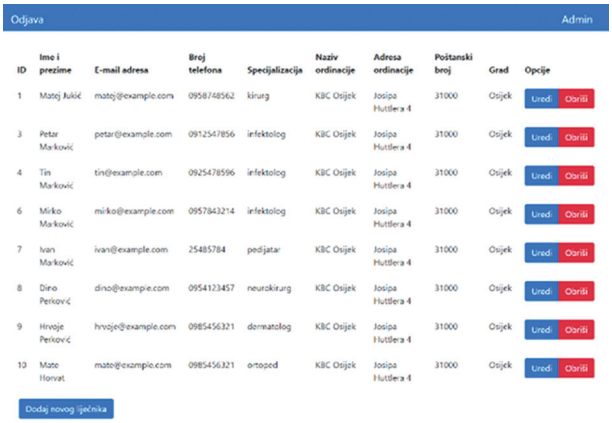

Fig. 8. Administrator profile page

4. CONCLUSION

In this paper an algorithm and online application for automatic appointment scheduling are presented. The application is implemented using the concept of booking patients' appointments for a specific service offered by individual medical staff. Primarily plan was to improve health tourism in Croatia by developing algorithm which will maximize doctor's efficiency and minimize patient waiting time. By maximizing efficiency patients will be more satisfied and have more services in selected time period. The algorithm is developed for that purpose and it allocates appointments to the database. The application itself is created in a Laravel which is used to build web applications based on MVC architecture. The layout scheme of the database was designed to contain all necessary data for the proper operation of the application. The main part of this paper is the development of the scheduling algorithm for multi/doctor and multi/patient system. The algorithm is designed to view the database and return an empty appointment which is appropriate for doctors and patients, remove overlaps and minimize waiting time. The application has two modes of user login, namely patients and doctors. Each has different functions and different views of the content, since they have different roles. Patients have been registered, logged in, selected, and scheduled appointments with the ability to edit their information, while doctors have been disabled from registering and added by the application administrator. Doctors have the ability to view scheduled appointments, add and delete individual services they offer, and edit their information. The response of the application is relatively fast, but after a while the amount of data in the database would increase and the speed would depend on the strength of the server. The problem could be solved by storing data in another memory location after a certain amount of time has elapsed since the end of the term. In future work we plan different improvements based on practical experience by using this application. We plan to assess doctors and patients to get feedback and find out possible improvements.

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ACKNOWLEDGMENTS

The paper is financed by project Optimization and scheduling in a dynamic system with multiple users and service providers.

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Commenced in 2010.
ISSN: 1847-6996
e-ISSN: 1847-7003

Published: semiannually

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